GENERAL DESCRIPTION

The MXC3500AL is an ultra-low power, low-noise, integrated digital output 3-axis accelerometer with a feature set optimized for wearables and consumer product motion sensing. Applications include wearable consumer products, IoT devices, user interface control, gaming motion input, electronic compass tilt compensation for cell phones, game controllers, remote controls, and portable media products.

Motion events: AnyMotion, Tilt, Flip, Shake, Single/Double/Triple Tap, Freefall, Six Degrees Orientation. Activity/Inactivity Detection, XYZ Magnitude.

In the MXC3500AL the internal sample rate can be set from 0.5 to 4000 samples / second. All Motion events or sample acquisition conditions can trigger an interrupt to a remote MCU. Alternatively, the device supports the reading of sample and event status via polling.

FEATURES

Range, Sampling & Power

- ±2, ±4, ±8, ±12, ±16, ±24 g range
- 16-bit sample resolution in ±24 g range
- 16-bit resolution with 1.5 Kbyte FIFO
- Sample rate 0.5 to 4000Hz
- 250nA @ 2Hz, Lowest power sniff
- 300nA @ 25Hz, Low power sniff
- 1.1 µA @ 25 Hz, Ultra-low power (ULP) mode
- 3µA @ 100 Hz, Low power (LP1) mode
- 5.8 µA @ 100 Hz, Low power/Low noise (LP2) mode
- 28 µA @ 1000Hz, Normal mode
- 40 µA @ 100Hz, Low noise mode

Simple System Integration

- SPI up to 10 MHz
- I2C interface, up to 1 MHz
- Integrated Temperature Sensor
- 2×2×0.73 mm 12-pin LGA package
- Low noise to 0.84mg RMS
- RoHS compliant

Applications

- Hearable & Wearables & IoT
- Smartphone
- Remote controls, VR & Game controllers

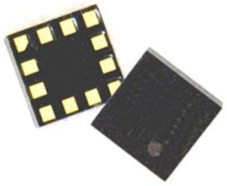


TABLE OF CONTENTS

1 ORDER INFORMATION

Table 1. Order Information

Part Number	Resolution	Order Number	Package	Shipping
MXC3500AL	16-bit	MXC3500AL	VLGA-12	Tape & Reel, 10Ku

Row	Marking
XXYM	Device identifier and date code
CCC	Factory lot code
●	Pin 1 identifier

Table 2. Package Information

2 FUNCTIONAL BLOCK DIAGRAM

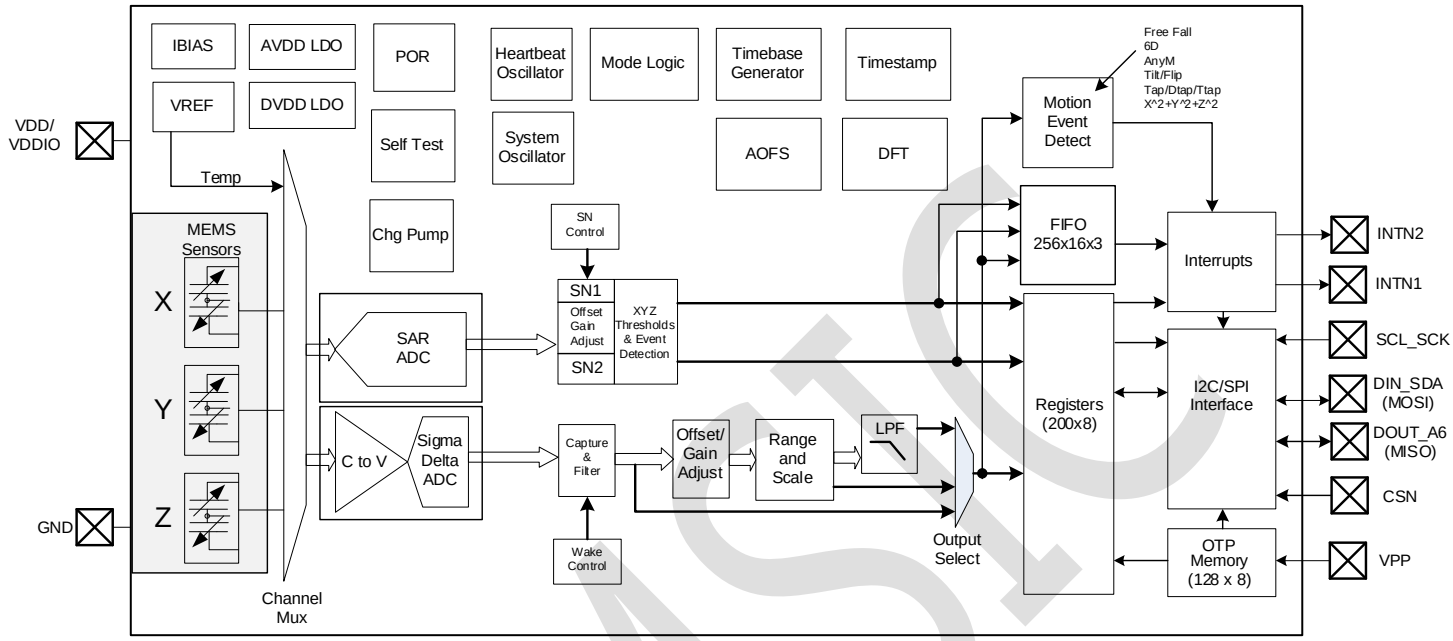
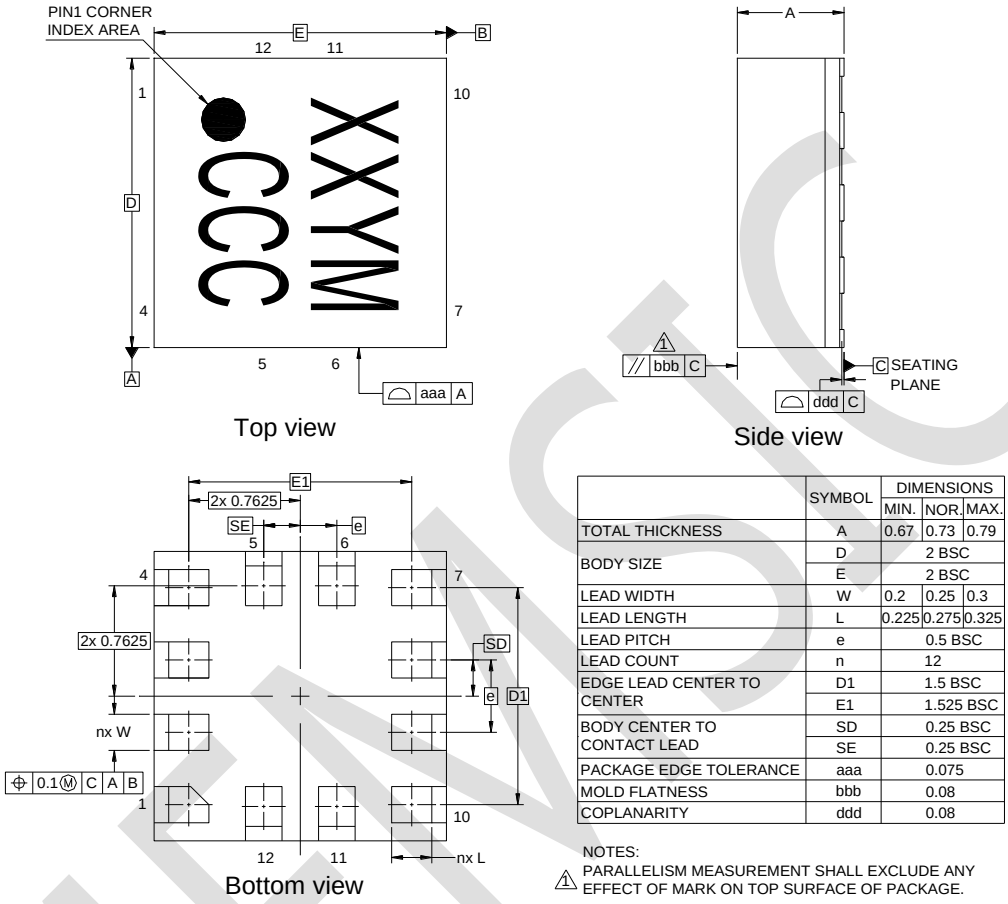


Figure 1. Block Diagram

3 PACKAGING AND PIN DESCRIPTION

3.1 PACKAGE OUTLINE



	SYMBOL	DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	0.67	0.73	0.79
BODY SIZE	D		2 BSC	
	E		2 BSC	
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.225	0.275	0.325
LEAD PITCH	e		0.5 BSC	
LEAD COUNT	n		12	
EDGE LEAD CENTER TO CENTER	D1		1.5 BSC	
	E1		1.525 BSC	
BODY CENTER TO CONTACT LEAD	SD		0.25 BSC	
	SE		0.25 BSC	
PACKAGE EDGE TOLERANCE	aaa		0.075	
MOLD FLATNESS	bbb		0.08	
COPLANARITY	ddd		0.08	

NOTES:
1. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 2. Package Outline and Mechanical Dimensions

3.2 PACKAGE ORIENTATION

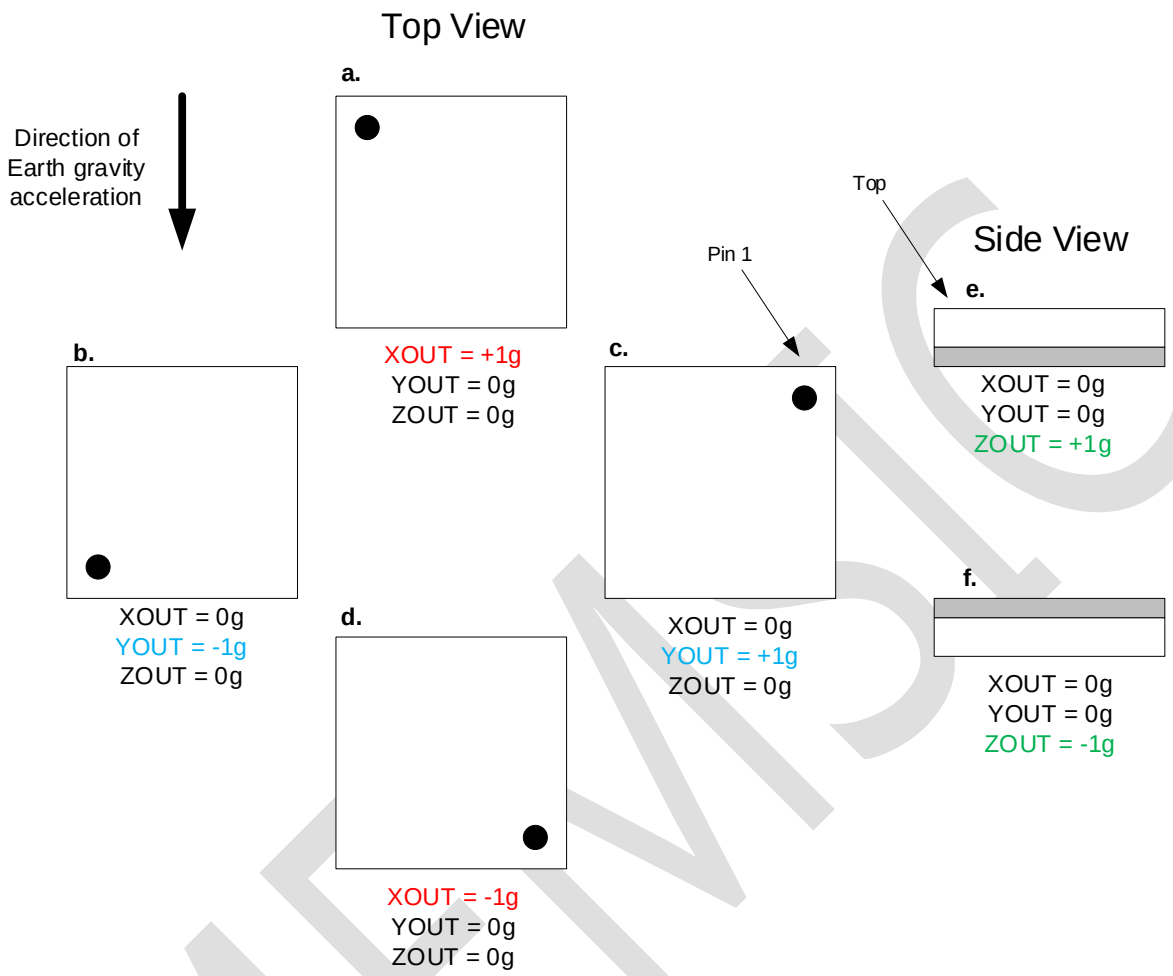


Figure 3. Package Orientation

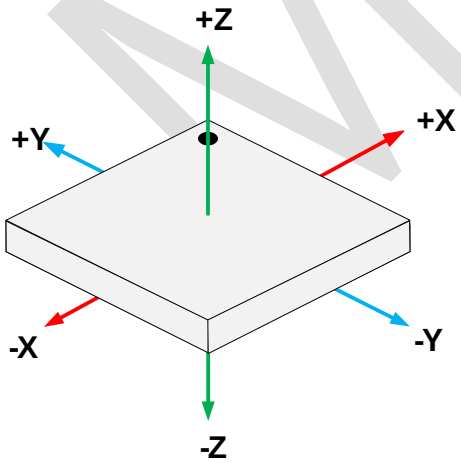


Figure 4. Package Axis Reference

3.3 MXC3500AL PIN DESCRIPTION

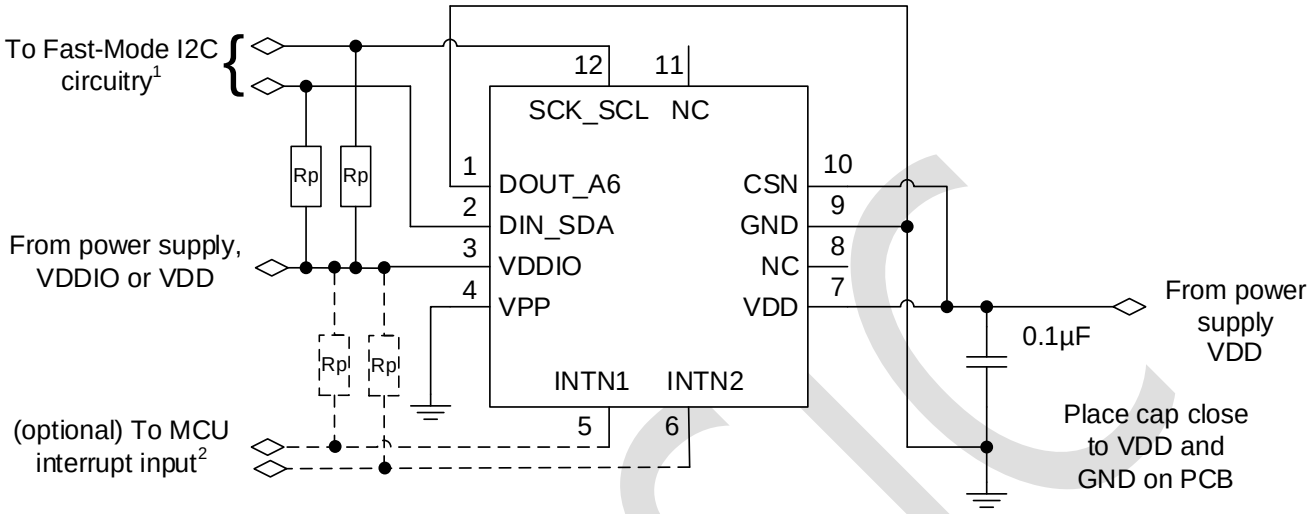
Pin	Name	Function
1	SDO/DOUT_A6	SPI data output Address select in I2C mode
2	SPI/SDA[1]	SPI data In I2C serial data input/output
3	VDDIO	Power supply for interface
4	VPP	Connect to GND
5	INT1[2]	Interrupt active LOW [3]
6	INT2[2]	Interrupt active LOW [3]
7	VDD	Power supply for internal
8	NC[4]	NC[4]
9	GND	Ground
10	CSN	SPI chip select (active low) I2C must connect to VDD
11	NC[4]	NC[4]
12	SCK/SCL[1]	SPI/I2C serial clock

Table 3. MXC3500AL Pin Description

Notes:

1) SCL and SDA require a pull-up resistor, typically 4.7kΩ to pin VDD. Refer to I2C Specification for Fast-Mode devices. Higher resistance values can be used (typically done to reduce current leakage) but such applications are outside the scope of this datasheet.
2) INT1/2 pins can be configured by software to operate either as an open-drain output or push-pull output (mode register). If set to open-drain, then it requires a pull-up resistor, typically 4.7kΩ to VDDIO or VDD.
3) INT1/2 pin polarity is programmable in the pad control register.
4) NC or “no connect” pins do not have any function on the MXC3500AL, and may be left unconnected, tied to GND, or tied to VDD.

3.4 MXC3500AL TYPICAL APPLICATION CIRCUITS

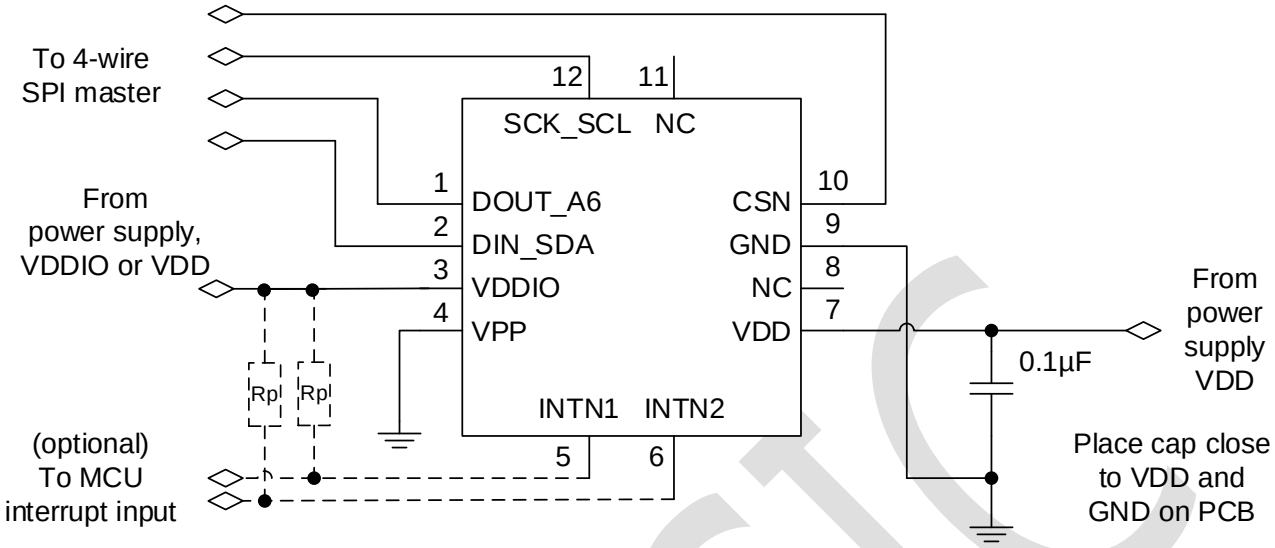


NOTE[1]: Rp are typically 4.7kΩ pullup resistors to VDDIO, per I2C specification. When VDDIO is powered down, DIN_SDA and SCK_SCL will be driven low by internal ESD diodes.

NOTE[2]: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

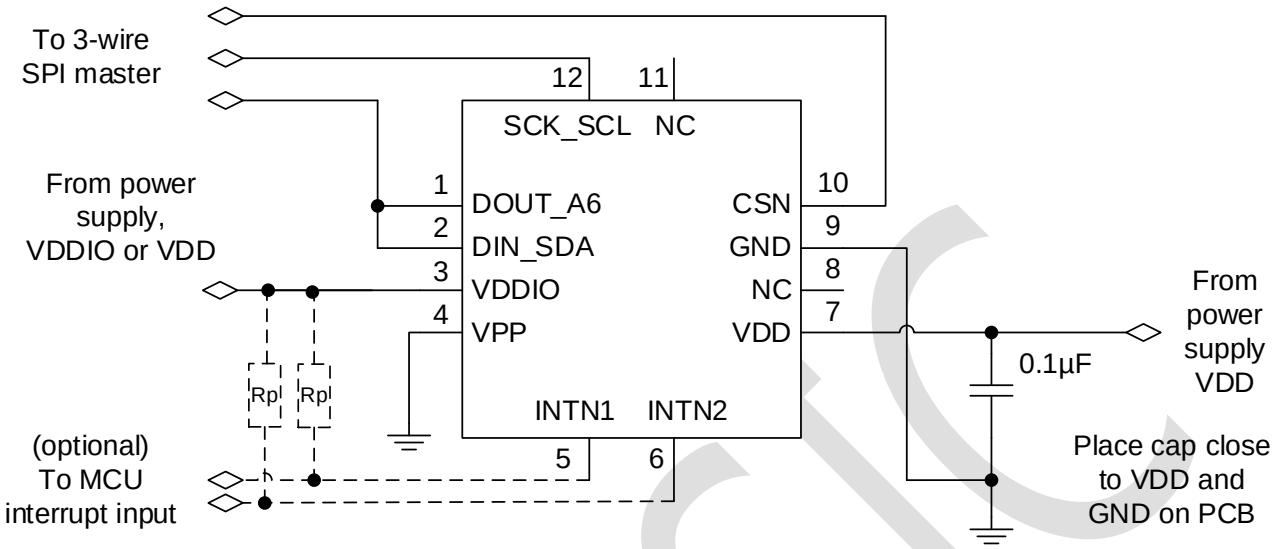
Figure 5. Typical I2C Application Circuit

In typical applications, the interface power supply may contain significant noise from external sources and other circuits which should be kept away from the sensor. Therefore, for some applications a lower-noise power supply might be desirable to power the VDD pin.



NOTE Rp: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

Figure 6. Typical 4-wire SPI Application Circuit

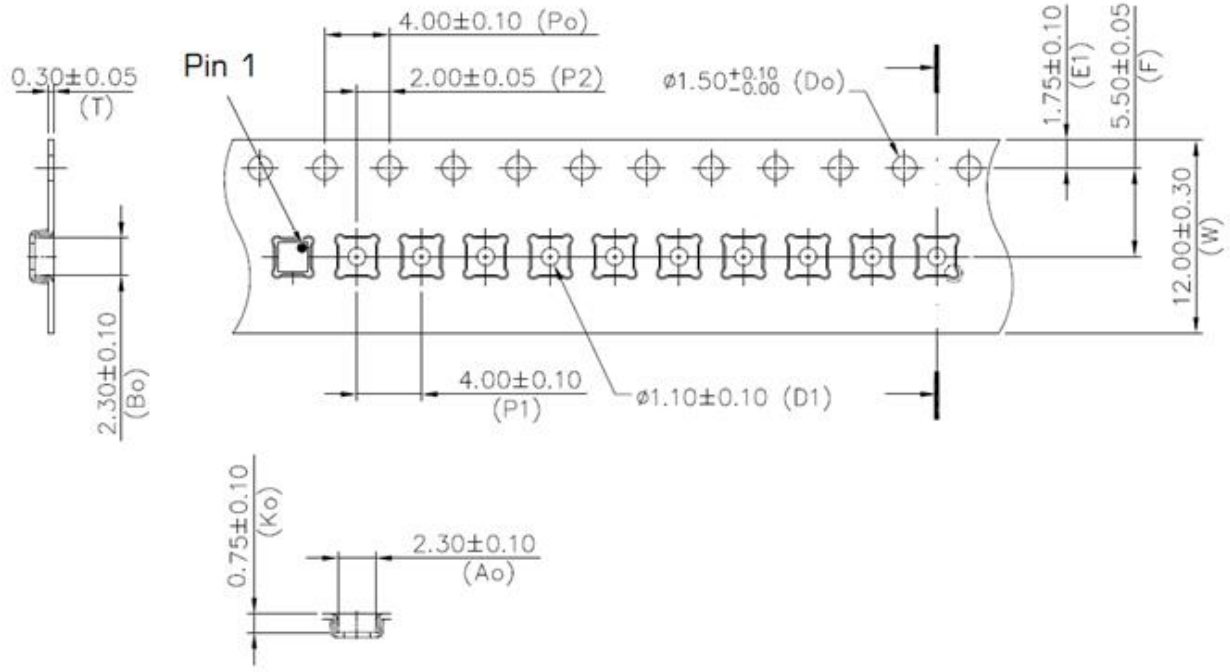


NOTE Rp: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

Figure 7. Typical 3-wire SPI Application Circuit

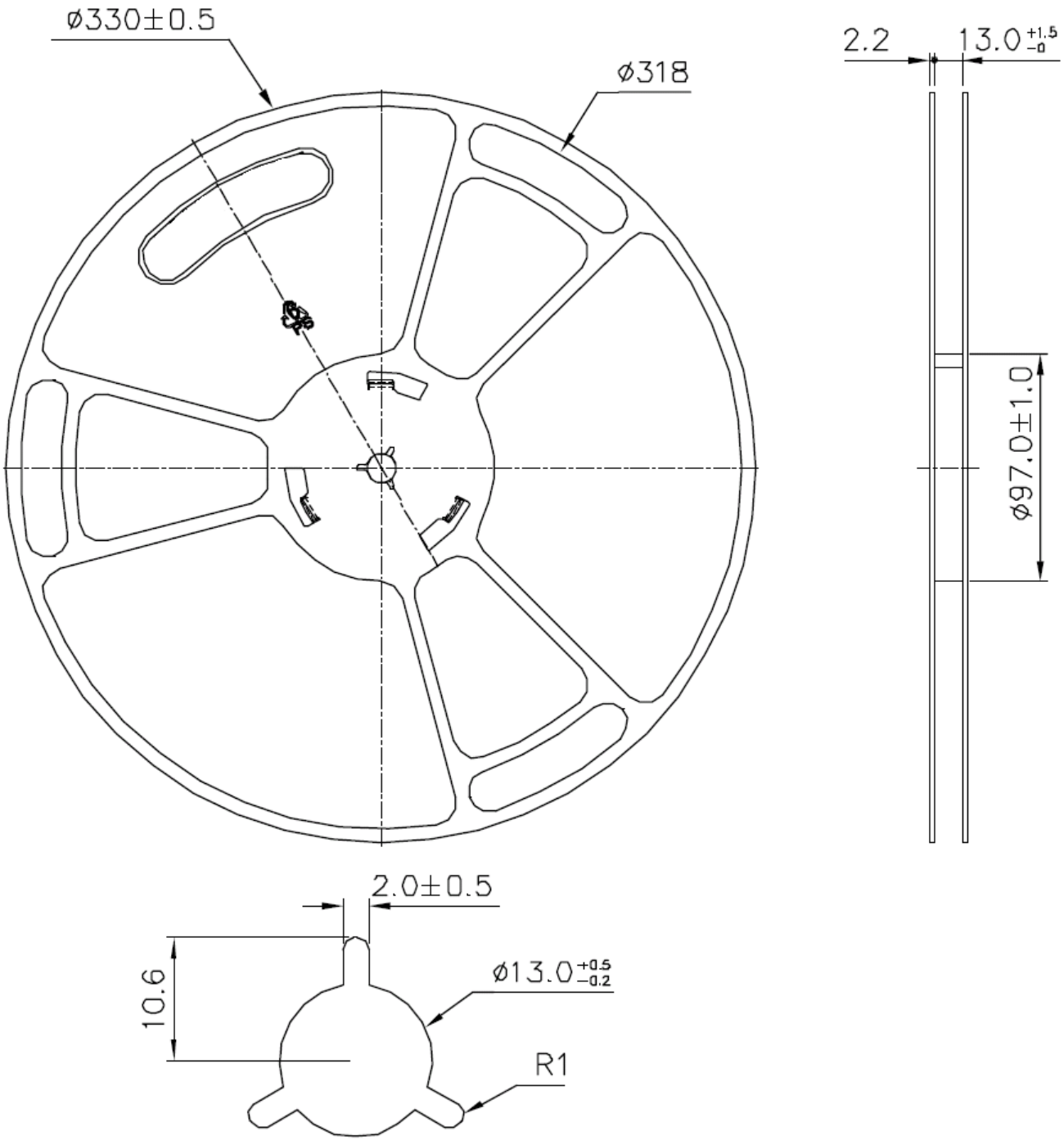
3.5 TAPE AND REEL

Devices are shipped in reels, in standard cardboard box packaging. See **Figure 8. MXC3500AL Tape Dimensions** and **Figure 9. MXC3500AL Reel Dimensions**.



- Dimensions in mm.
- 10 sprocket hole pitch cumulative tolerance ±0.2
- Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Figure 8. MXC3500AL Tape Dimensions



- Dimensions in mm.

Figure 9. MXC3500AL Reel Dimensions

3.6 SOLDERING PROFILE

The LGA package follows the reflow soldering classification profiles described in *Joint Industry Standard, Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices*, document number J-STD-020E. Reflow soldering has a peak temperature (T_p) of 260ºC

3.7 SHIPPING AND HANDLING GUIDELINES

Shipping and handling follow the standards described in *Joint Industry Standard, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*, document number J-STD-033C.

The following are additional handling guidelines (refer to the MEMSIC document, PCB Design, Device Handling and Assembly Guidelines, for more information):

- While the mechanical sensor is designed to handle high-g shock events, direct mechanical shock to the package should be avoided.
- SMT assembly houses should use automated assembly equipment with either plastic nozzles or nozzles with compliant tips (for example, soft rubber or silicone).
- Avoid g-forces beyond the specified limits during transportation.
- Handling and mounting of sensors should be done in a defined and qualified installation.

3.8 MOISTURE SENSITIVITY LEVEL CONTROL

The following are storage recommendations (refer to the MEMSIC document, PCB Design, Device Handling and Assembly Guidelines, for more information):

- Store the tape and reel in the *unopened* dry pack, until required on the assembly floor.
- If the dry pack has been opened or the reel has been removed from the dry pack, reseal the reel inside of the dry pack with a black protective belt. Avoid crushing the tape and reel.
- Store the cardboard box in a vertical position.

4 SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Parameters exceeding the Absolute Maximum Ratings may permanently damage the device.

Rating	Symbol	Minimum / Maximum Value	Unit
Supply Voltages	Pin VDD	-0.3 / 3.6	V
Acceleration, any axis, 100*μs*	g_{max}	10000	g
Ambient operating temperature	T_{OP}	-40 / +85	ºC
Storage temperature	T_{STG}	-40 / +125	ºC
ESD human body model	HBM	± 2000	V
Latch-up current at T_{op} = 25 ºC	I_{LU}	100	mA
Input voltage to non-power pin	Pins SDA, INTN and SCK	-0.3 / (VDD + 0.3) or 3.6 whichever is lower	V

Table 4. Absolute Maximum Ratings

4.2 SENSOR CHARACTERISTICS

VDD = 1.2V, VDDIO = 1.65V, T_{op} = 25 ºC for LP1, LP2, Normal and ULP modes unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Acceleration range			±2.0 ±4.0 ±8.0 ±12.0 ±16.0 ±24.0		g
Sensitivity	Acceleration range = ±2.0g		16384		LSB/g
	Acceleration range = ±4.0g		8192		
	Acceleration range = ±8.0g		4096		
	Acceleration range = ±12.0g		2730		
	Acceleration range = ±16.0g		2048		
	Acceleration range = ±24.0g		1365		
Sensitivity Temperature Coefficient [1]	-40 ºC ≤ T_{op} ≤ +85 ºC		±0.015		%/ºC
Zero-g Offset	Chip Level Board Level Mode Change [(2)]		±20 ±40 < ±60		mg
Zero-g Offset Temperature Coefficient [1]	-40 ºC ≤ T_{op} ≤ +85 ºC		±0.5		mg/ºC
Noise Density [1]	Ultra low noise (ULN) mode		0.84(XY) 1.7(Z)		mg rms
Nonlinearity [1]	Acceleration range = ±1.0g		0.65 (XY) 1.0 (Z)		% FS
Cross-axis Sensitivity [1]	Between any two axes		±1		%
ODR, Output Data Rate		0.5		4000[3]	Hz

[1] Values are based on device characterization and are not tested in production.

[2] Mode change is defined as a major change in sampling precision (e.g. LP to ULP mode)

[3] ULN mode with ODR = 4000Hz (registers x25 = x58, x26 = x02, x27 = x00, x54 = x00)

Table 5. Sensor Characteristics

4.3 ELECTRICAL AND TIMING CHARACTERISTICS

4.3.1 ELECTRICAL POWER AND INTERNAL CHARACTERISTICS

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Supply voltage [1]	Pin VDD Rise-Time < 50mSec	VDD	1.14		3.6	V
Supply voltage [1]	Pin VDDIO Rise-Time < 50mSec	VDDIO	1.62		3.6	V
Sample Rate (ODR) Tolerance [2]		Tclock	-2		2	%

[1] Min and Max limits are hard limits without additional tolerance.

[2] Values are based on device design and not characterized or tested in production.

Test condition: VDD = 1.2V, VDDIO = 1.65V, T_{op} = 25 ºC unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Standby Current	Sleep Mode		100		nA
SNIFF, Lowest Power	SNIFF Mode, 2 Hz		250		nA
SNIFF, Low Power	SNIFF Mode, 25 Hz		300		nA
WAKE, ULP	WAKE Mode, 10 Hz(without FIFO) 10Hz (with FIFO ON) WAKE Mode, 25 Hz(FIFO)		0.8 0.85 1.1		µA
WAKE, LP1	Low Power Mode 1, ODR = 100 Hz		3		µA
WAKE, LP2	Low Power Mode 2 /Low Noise ODR = 100 Hz		5.8		µA
WAKE, Normal	ODR = 1000 Hz		28		µA
WAKE, Low Noise (LN) Mode[1]	ODR = 100 Hz VDD = 1.8V		40		µA
WAKE, Ultra Low Noise (ULN) Mode[1]	ODR = 100 Hz VDD = 1.8V		150		µA
Pad Leakage[2]	Per I/O pad	-1	0.01	1	µA
Wake-Up time[2]			2		ms
Start-Up time[2]			1/ODR+1 mS		ms

[1]Values are based on device characterization and not tested in production.

[1]Values are based on device design and not characterized or tested in production.

Table 6. Electrical Characteristics

4.3.2 ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
LOW level input voltage	VIL	-0.5	0.3* VDDIO	V
HIGH level input voltage	VIH	0.7*VDDIO	-	V
Hysteresis of Schmitt trigger inputs	Vhys	0.05*VDDIO	-	V
Output voltage, pin INTN 1 or INTN 2, Iol ≤ 2 mA	Vol Voh	0 0	0.4 0.9* VDDIO	V V
Output voltage, pin DIN_SDA (open drain), Iol ≤ 1 mA	Vols	-	0.1* VDDIO	V
Input current, pins DIN_SDA and SCK_SCL (input voltage between 0.1* VDDIO and 0.9* VDDIO max)	Ii	-10	10	µA
Capacitance, pins DIN_SDA and SCL [1]	Ci	-	10	pF
Values are based on device design and not characterized or tested in production.				

Table 7. Electrical and Timing Characteristics - Interface

NOTES:

- If multiple slaves are connected to the I2C signals in addition to this device, only 1 pull-up resistor on each of SDA and SCK should exist. Also, care must be taken to not violate the I2C specification for capacitive loading.
- When pin VDD is disconnected from power or ground (e.g. Hi-Z), the device may become inadvertently powered up through the ESD diodes present on other powered signals.

4.3.3 I2C TIMING CHARACTERISTICS

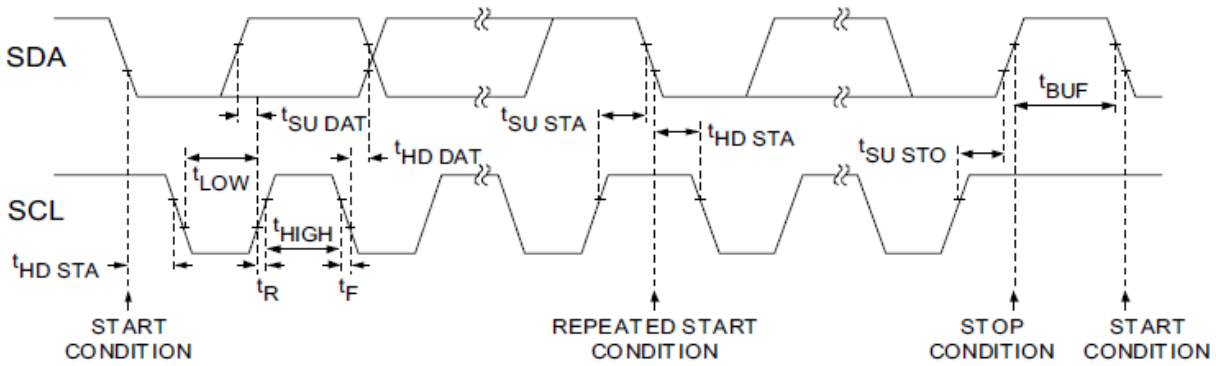


Figure 10. I2C Interface Timing

Parameter	Description	Standard Mode		Fast Mode		Fast Mode Plus		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	Data hold time	5.0	-	-	-	-	-	µs
$t_{SU;DAT}$	Data set-up time	250	-	100	-	50	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START	4.7	-	1.3	-	0.5	-	µs

Table 8. I2C Timing Characteristics

NOTE: Values are based on I2C Specification requirements, not tested in production.

4.3.4 SPI TIMING CHARACTERISTICS

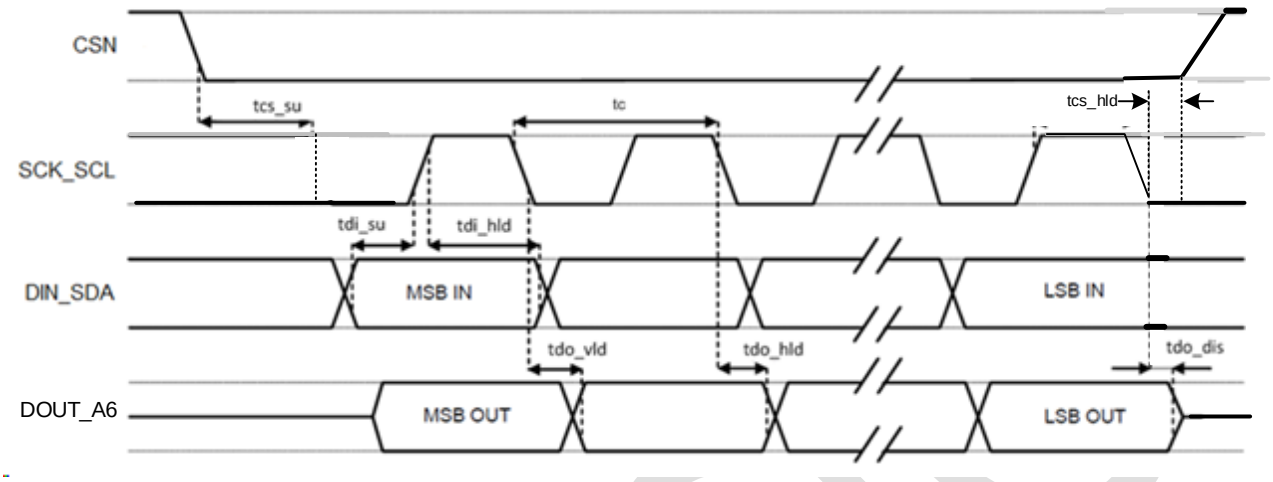


Figure 11. SPI Interface Timing Waveform (Mode 0)

Symbol	Parameter	Value		Units
		Min	Max	
tc	SPI SCK_SCL Clock Cycle	100		ns
fc	SPI SCK_SCL Clock Frequency		10	MHz
tcs_su	SPI CSN Setup Time	6		ns
tcs_hld	SPI CSN Hold Time	8		ns
tdi_su	SPI DIN_SDA Input Setup Time	5		ns
tdi_hld	SPI DIN_SDA Input Hold Time	15		ns
tdo_vld	SPI DOUT_A6 Valid Output Time		50	ns
tdo_hld	SPI DOUT_A6 Output Hold Time	9		ns
tdo_dis	SPI DOUT_A6 Output Disable Time		50	ns

Table 9. SPI Interface Timing Parameters

5 GENERAL OPERATION

The MXC3500AL is a three-axis accelerometer design. The architecture is two ADCs (SAR and SDM) and two data piplines, SNIFF and WAKE, with digital gain and offset correction. The WAKE mode operational range is ± 2/4/8/12/16/24g at resolution of 16-bits. Configuration and control are via an I2C or SPI slave interface. A non-volatile memory (OTP) retains device and calibration parameters.

The SAR (successive approximation) ADC supports very low power sampling using the SNIFF mode pipeline. A temperature sensor is read using the SAR. The 16-bit SDM (sigma-delta) ADC supports higher power and faster data rates using the WAKE mode pipeline. A 256 sample x 16-bit x 3 channel FIFO can be used to capture data. The FIFO supports burst (read) and stream (overwrite) operations and has three interrupts.

MXC3500AL has a a “smart” state machine for power management. The Mode state machine can switch between the low power SNIFF and higher power WAKE states based on activity/inactivity levels. The MXC3500AL features a motion block which implements algorithms to support many detection features such as “AnyMotion”, “Shake”, “Tilt/Flip”, “Tap/Double Tap/Triple Tap”, “6D Orientation”, and “Freefall”.

5.1 SENSOR SAMPLING

5.1.1 SNIFF MODE SAMPLING

The MXC3500AL has dedicated SNIFF logic to detect events and very low data rates and power. Typical sampling rates are between 2 Hz and 50 Hz. The SNIFF mode sampling uses the 8-bit SAR ADC. Digital gain and offset correction are applied to the SNIFF samples. User programmable parameters for SNIFF detection are based on X, Y, and Z thresholds and detection counts.

SNIFF Mode 1 (SN1) is the lowest power mode, and SNIFF Mode 2 (SN2) supports seamless transitions between SNIFF and WAKE modes based on activity/inactivity.

New SNIFF samples are compared to previous samples. Comparison modes are:
(1) Comparing the current sample to a user programmed value (current to baseline).

(2) The first sample taken when entering SNIFF (first to current).

(3) The ‘immediate’ previous sample (current to previous).

When SNIFF activity is detected the MXC3500AL will issue an optional WAKEUP interrupt and move to WAKE mode.

5.1.2 WAKE MODE SAMPLING

MXC3500AL WAKE mode supports sampling rates up to 4000 kHz. A full featured motion detection suite, 2nd Butterworth low pass filter, and FIFO are available in WAKE mode. The WAKE mode pipeline uses the 16-bit SDM ADC. Digital gain and offset correction are applied to WAKE samples and the output is written to the X, Y, Z registers as a 16-bit 2's compliment number.

The motion detection features are "AnyMotion", "Shake", "Tilt/Flip", "Tap/Double Tap/Triple Tap", "6D Orientation", and "Freefall". Each motion feature supports a dedicated interrupt which may be assigned to the INT1 or INT2 pads.

WAKE mode supports inactivity detection and will move to SNIFF mode when the detection threshold and duration are met.

5.2 OFFSET AND GAIN CALIBRATION

The default digital offset and gain calibration data can be read from the device, if necessary, to reduce the effects of post-assembly influences and stresses which may cause the sensor readings to be offset from their factory values.

5.3 RESET OR INITIALIZATION

The MXC3500AL can be completely reset via an I2C or SPI instruction. Writing register 0x7F with 0x80 (bit 7) causes a power-on reset operation to execute. No attempt should be made to access registers within 2mSec after issuing this operation. The pin DOUT_A6 is sampled for the purposes of setting the I2C device address after this reset operation.

NOTE: Immediately after a RESET or power-up event, software will read the following registers to confirm the MXC3500AL is ready to accept initialization.

NOTE: Memsic will provide additional information pending MXC3500AL charactrerization.

Step	Address	Value to be read	Comment
1	0x00	0xF0	Confirm MXC3500AL Memsic family ID
2	0x01	0x01	Confirm MXC3500AL Memsic version ID
3	0x02	0x42	MXC3500AL boot is complete and ready to accept register commands/ initialization (Bit 6 = BOOT_DONE, Bits 3:0 = 0x2 is the Mode state machine 'SLEEP' state).
4	Configure remaining registers and use sensor as normal.		

Table 10: MXC3500AL Initialization Sequence for I2C and SPI Intrerfaces

5.4 OPERATIONAL STATES

The MXC3500AL responds to four different software commands written to register 0x14 bits 2:0, the STATE[2:0] bits. The following operational modes are supported.

Register 0x14 Bits [2:0]	MODE/STATE	Description
000	SLEEP	• SLEEP is the default state once the device completes a POR or software reset.
001	SN1	• SN1 is the lowest power SNIFF state. In this mode all other features are OFF. • SN1 SNIFF uses the SAR ADC for sampling. Digital offset and gain correction are applied to samples. • Three independent X/Y/Z programmable thresholds are used to determine if a WAKEUP event is detected. • **Stay in SN1**: SN1 normally moves to the WAKE state upon detecting a valid event. If the device is to stay in the SN1 state, use the SN1_FREEZE bit in register 0x14 bit 3. This will keep the device sampling in the lower power SN1 state. • **WAKEUP**: As the lowest power state, all registers required for WAKE mode operation **must** be configured after the WAKEUP event. On WAKEUP, the state machine will move to the WAIT_WAKE_PGM_DONE state for WAKE mode register programming.
010	SN2	• SN2 is the higher power SNIFF state. • SN2 SNIFF uses the SAR ADC for sampling. Digital offset and gain correction are applied to samples. Three independent X/Y/Z programmable thresholds are used to determine if a WAKEUP event is detected. • SN2 supports XYZ threshold event counts (see registers 0x21,0x22,0x23). This feature is not available in SN1.

		• **Stay in SN2**: SN2 normally moves to the WAKE state upon detecting a valid event. If the device is to stay in the SN2 state, use the SN2_FREEZE bit in register 0x14 bit 4. This will keep the device sampling in the lower power SN2 state. • **WAKEUP:** As the higher power SNIFF state, all registers required for WAKE mode are to be configured before entering SN2 SNIFF mode. This allows for all required WAKE mode settings to be ready immediately on a valid WAKEUP event.
001	WAKE	• WAKE mode is the highest power state. In this mode all features are on. • WAKE mode uses the SDM ADC for sampling. Digital offset and gain correction are applied to samples. • The low pass filter, all motion detection features, interrupts, and the FIFO are available for use. • SN1 or SN2 may auto-transition to the WAKE state on WAKEUP event. Optionally, the INACTIVITY feature may be used to auto-transition back to SN2 mode once no additional activity has been detected.
100 101 110 111	STATE[2:0]	• Reserved

Table 11: Operational States

5.5 MODE OPERATIONAL FLOW

The figure below shows the overall operational state flow for the MXC3500AL. The device defaults to SLEEP following power-on. Mode transitions occur at typical rate of 10 kHz (as set in register 0x1E).

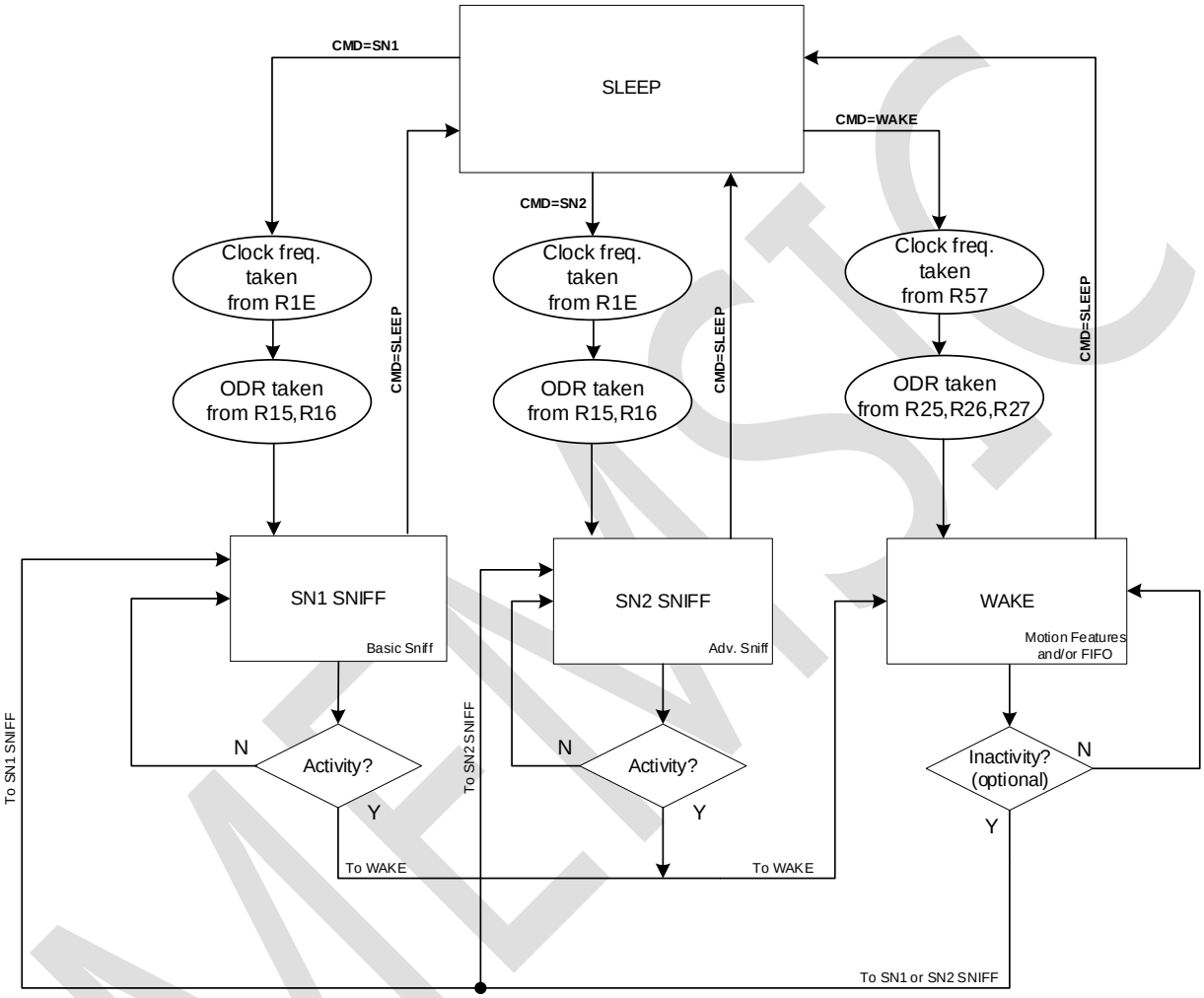


Figure 12: Operational State Flow

Figure 13 below the full Mode state machine flow for the MXC3500AL; this is more detailed than figure Figure 12. The MXC3500AL always arrives at the SLEEP state following a POR or SW_RESET. For SN2 SNIFF and WAKE (as set by register 0x14 [2:0]), hardware checks that the local power is enabled (“good”) and then waits for software to configure all necessary registers. Once register programming is finished, software sets PRG_DONE at register 0x24 bit 7 to being samping in SN2 SNIFF or WAKE modes.

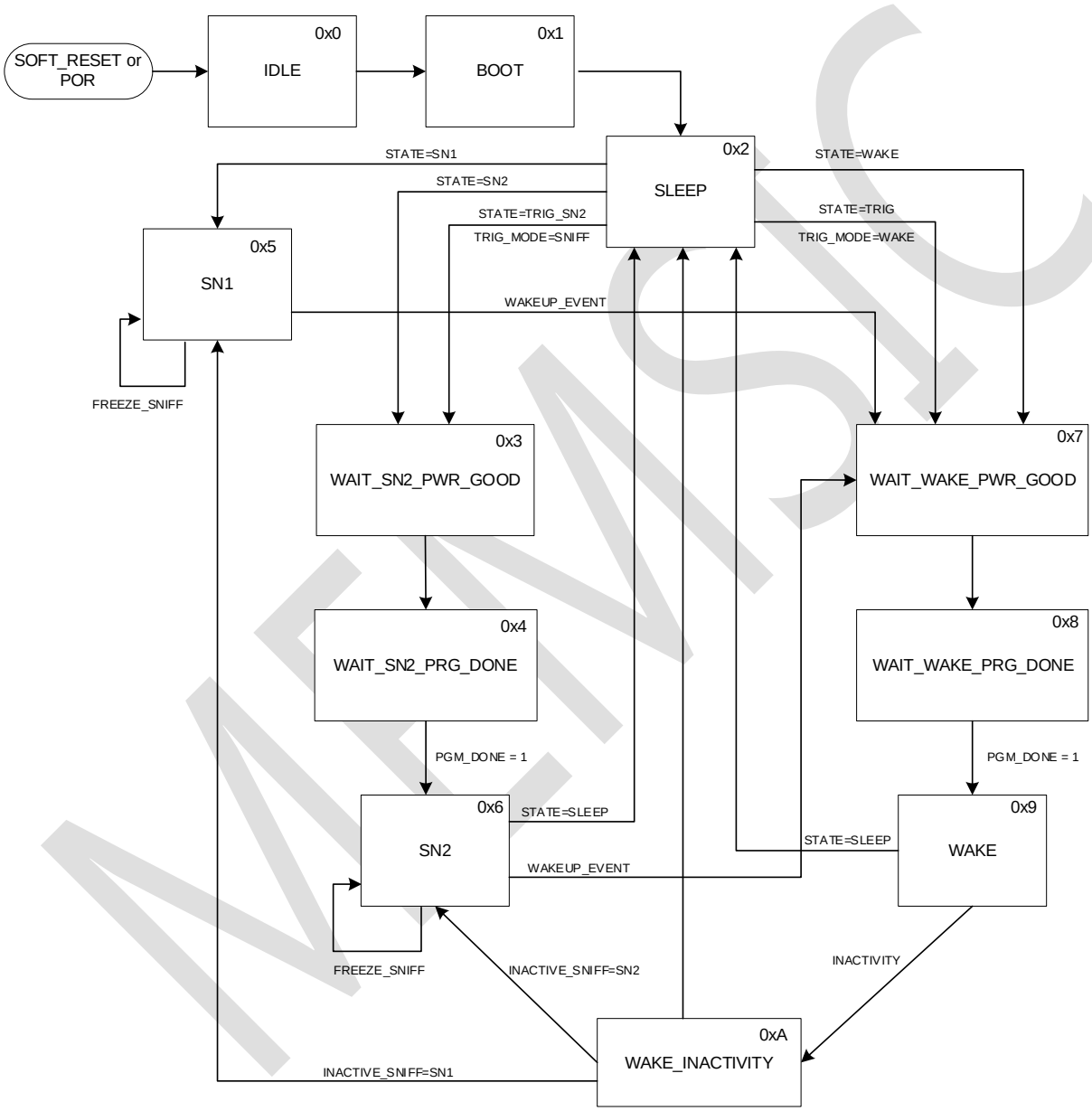


Figure 13: Mode State Machine Flow

5.6 MODE SWITCHING

In order to switch from one wake mode to another one, please follow this procedure.

5.6.1 LP1 SETTINGS

Write x14=x00 (not necessary if switching from sleep mode)

Delay 10ms (not necessary if switching from sleep mode)

Write x11=x03

Write x14=x03

READ x02 until it's x48 (check for 100 times, if x02 is still =x42, please write x7F=x80 and restart from the top)

Write x55=x00 (or other desired g-range)

Write x20=xC0

Write x57=x06

Write x54=x00

Write x56=x08

Write x59=x71

Write x25=x78

Write x26=x01

Write x24=xC3

Write xB6=x00

Write xB7=x12

Write x94=x11

LPF settings (optional):

Write x64=x7E

Write x65=x25

Write x66=xFB

Write x67=x4A

Write x68=x7E

Write x69=x25

Write x6A=x00

Write x6B=x00

Write x6C=xF6

Write x6D=x15

Write x6E=x01

Below section is optional, if the part is freshly powered-up, soft-reset, or writes to registers x80-x85 never happened.

Also, LP1 Values#0 – 5 can be recorded beforehand (for example, at system initialization) and stored in MCU memory for later use, so that the script below is simplified to writing LP1 Values#0 – 5 into registers x80-x85.

Write x7A=x80

Write x78=x12

Write x79=x00

Write x7B=x00

Write x7A=x88

Write x7A=x80

Write x7B=x00

READ x7D= LP1 Value#0

Write x7A=x00

Delay 1ms

Write x80= LP1 Value#0

Write x7A=x80

Write x78=x12

Write x79=x00

Delay 10ms

Write x7B=x00

Write x7A=x88

Write x7A=x80

Write x7B=x01

READ x7D= LP1 Value#1

Write x7A=x00

Delay 1ms

Write x81= LP1 Value#1

Write x7A=x80

Write x78=x12

Write x79=x00

Delay 1ms
Write x7B=x00
Write x7A=x88
Write x7A=x80
Write x7B=x02
READ x7D= LP1 Value#2
Write x7A=x00
Delay 1ms
Write x82= LP1 Value#2

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B=x00
Write x7A=x88
Write x7A=x80
Write x7B=x03
READ x7D= LP1 Value#3
Write x7A=x00
Delay 1ms
Write x83= LP1 Value#3

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 1ms
Write x7B=x00
Write x7A=x88
Write x7A=x80
Write x7B=x04
READ x7D= LP1 Value#4
Write x7A=x00

Delay 1ms

Write x84= LP1 Value#4

Write x7A=x80

Write x78=x12

Write x79=x00

Delay 1ms

Write x7B=x00

Write x7A=x88

Write x7A=x80

Write x7B=x05

READ x7D= LP1 Value#5

Write x7A=x00

Delay 1ms

Write x85= LP1 Value#5

5.6.2 LP2 SETTINGS

Write x14=x00 (not necessary if switching from sleep mode)

Delay 10ms (not necessary if switching from sleep mode)

Write x11=x03

Write x14=x03

READ x02 until it's x48 (check for 100 times, if x02 is still =x42, please write x7F=x80 and restart from the top)

Write x55=x00 (or other desired g-range)

Write x20=xC0

Write x57=x05

Write x54=x01

Write x56=x08

Write x59=xA0

Write x25=xDC

Write x26=x02

Write x24=xC3

Write xB6=x02

Write xB7=x12

Write x94=x11

LPF settings (optional):

Write x64=x7E

Write x65=x25

Write x66=xFB

Write x67=x4A

Write x68=x7E

Write x69=x25

Write x6A=x00

Write x6B=x00

Write x6C=xF6

Write x6D=x15

Write x6E=x01

Below section is optional, if LP2 Values#0-5 were already written to the registers x80-x85, and the part was NOT power-cycled or soft-reset since then

Also, LP2 Values#0-5 can be recorded beforehand (for example, at system initialization) and stored in MCU memory for later use, so that the script below is simplified to writing LP2 Values#0-5 into registers x80-x85

Write x7A=x80

Write x78=x12

Write x79=x00

Delay 10ms

Write x7B=x20

Write x7A=x88

Write x7A=x80

Write x7B=x24

READ x7D= LP2 Value#0

Write x7A=x00

Delay 10ms

Write x80= LP2 Value#0

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B=x20
Write x7A=x88
Write x7A=x80
Write x7B=x25
READ x7D= LP2 Value#1
Write x7A=x00
Delay 10ms
Write x81= LP2 Value#1

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B=x20
Write x7A=x88
Write x7A=x80
Write x7B=x26
READ x7D= LP2 Value#2
Write x7A=x00
Delay 10ms
Write x82= LP2 Value#2

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B=x20
Write x7A=x88
Write x7A=x80

Write x7B=x27
READ x7D= LP2 Value#3
Write x7A=x00
Delay 10ms
Write x83= LP2 Value#3

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B=x28
Write x7A=x88
Write x7A=x80
Write x7B=x28
READ x7D= LP2 Value#4
Write x7A=x00
Delay 10ms
Write x84= LP2 Value#4

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B=x28
Write x7A=x88
Write x7A=x80
Write x7B=x29
READ x7D= LP2 Value#5
Write x7A=x00
Delay 10ms
Write x85= LP2 Value#5

5.6.3 NORMAL SETTINGS

Write x14=x00 (not necessary if switching from sleep mode)

Delay 10ms (not necessary if switching from sleep mode)

Write x11=x03

Write x14=x03

READ x02 until it's x48 (check for 100 times, if x02 is still =x42, please write x7F=x80 and restart from the top)

Write x55=x00 (or other desired g-range)

Write x20=xC0

Write x57=x0C

Write x54=x00

Write x56=x08

Write x59=x71

Write x25=xDC

Write x26=x02

Write x24=xC3

Write xB6=x0E

Write xB7=x16

Write x94=x11

READ x9F VALUE

Write x9F=VALUE+2

When swithing from Normal mode to any other mode,

WRITE x9F=VALUE

LPF settings (optional):

Write x64=xB6

Write x65=x00

Write x66=x6B

Write x67=x01

Write x68=xB6

Write x69=x00

Write x6A=xAA

Write x6B=xE3

Write x6C=x81

Write x6D=x66

Write x6E=x01

Below section is optional, if Normal Values#0-5 were already written to the registers x80-x85, and the part was NOT power-cycled or soft-reset since then

Also, Normal Values#0-5 can be recorded beforehand (for example, at system initialization) and stored in MCU memory for later use, so that the script below is simplified to writing Normal Values#0-5 into registers x80-x85

Write x7A=x80

Write x78=x12

Write x79=x00

Delay 10ms

Write x7B=x28

Write x7A=x88

Write x7A=x80

Write x7B=x2A

READ x7D= Normal Value#0

Write x7A=x00

Delay 10ms

Write x80= Normal Value#0

Write x7A=x80

Write x78=x12

Write x79=x00

Delay 10ms

Write x7B=x28

Write x7A=x88

Write x7A=x80

Write x7B=x2B

READ x7D= Normal Value#1

Write x7A=x00

Delay 10ms
Write x81= Normal Value#1

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B=x28
Write x7A=x88
Write x7A=x80
Write x7B=x2C
READ x7D= Normal Value#2
Write x7A=x00
Delay 10ms
Write x82= Normal Value#2

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B=x28
Write x7A=x88
Write x7A=x80
Write x7B=x2D
READ x7D= Normal Value#3
Write x7A=x00
Delay 10ms
Write x83= Normal Value#3

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms

Write x7B=x28

Write x7A=x88

Write x7A=x80

Write x7B=x2E

READ x7D= Normal Value#4

Write x7A=x00

Delay 10ms

Write x84= Normal Value#4

Write x7A=x80

Write x78=x12

Write x79=x00

Delay 10ms

Write x7B=x28

Write x7A=x88

Write x7A=x80

Write x7B=x2F

READ x7D= Normal Value#5

Write x7A=x00

Delay 10ms

Write x85= Normal Value#5

5.6.4 ULP SETTINGS

Write x14=x00 (not necessary if switching from sleep mode)

Delay 10ms (not necessary if switching from sleep mode)

Write x11=x03

Write x14=x03

READ x02 until it's x48 (check for 100 times, if x02 is still =x42, please write x7F=x80 and restart from the top)

Write x55=x00 (or other desired g-range)

Write x20=xC0

Write x57=x03

Write x54=x00

Write x56=x08

Write x59=x71

Write x25=xF4

Write x26=x01

Write x24=xC3

Write xB6=x00

Write xB7=xD2

Write x94=x11

READ x9E VALUE

If VALUE = 7 Then NEW_VALUE = 10

Else NEW_VALUE = VALUE + 1

Write x9E NEW_VALUE

When swithing from ULP mode to any other mode,

WRITE x9E=VALUE

LPF settings (optional):

Write x64=x7E

Write x65=x25

Write x66=xFB

Write x67=x4A

Write x68=x7E

Write x69=x25

Write x6A=x00

Write x6B=x00

Write x6C=xF6

Write x6D=x15

Write x6E=x01

Below section is optional, if ULP Values#0-5 were already written to the registers x80-x85, and the part was NOT power-cycled or soft-reset since then

Also, ULP Values#0-5 can be recorded beforehand (for example, at system initialization) and stored in MCU memory for later use, so that the script below is simplified to writing ULP Values#0-5 into registers x80-x85

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B=x30
Write x7A=x88
Write x7A=x80
Write x7B=x30
READ x7D= ULP Value#0
Write x7A=x00
Delay 10ms
Write x80= ULP Value#0

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B=x30
Write x7A=x88
Write x7A=x80
Write x7B=x31
READ x7D= ULP Value#1
Write x7A=x00
Delay 10ms
Write x81= ULP Value#1

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B= x30
Write x7A=x88

Write x7A=x80
Write x7B= x32
READ x7D= ULP Value#2
Write x7A=x00
Delay 10ms
Write x82= ULP Value#2

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B= x30
Write x7A=x88
Write x7A=x80
Write x7B= x33
READ x7D= ULP Value#3
Write x7A=x00
Delay 10ms
Write x83= ULP Value#3

Write x7A=x80
Write x78=x12
Write x79=x00
Delay 10ms
Write x7B= x30
Write x7A=x88
Write x7A=x80
Write x7B= x34
READ x7D= ULP Value#4
Write x7A=x00
Delay 10ms
Write x84= ULP Value#4

Write x7A=x80

Write x78=x12

Write x79=x00

Delay 10ms

Write x7B= x30

Write x7A=x88

Write x7A=x80

Write x7B= x35

READ x7D= ULP Value#5

Write x7A=x00

Delay 10ms

Write x85= ULP Value#5

5.6.5 LOW NOISE (LN) SETTINGS

This mode must be used with VDD >=1.8V

This mode is not tested in production and may have offsets and sensitivity errors higher than specified in the tables above.

Write x14=x00 (not necessary if switching from sleep mode)

Delay 10ms (not necessary if switching from sleep mode)

Write x11=x03

Write x14=x03

READ x02 until it's x48 (check for 100 times, if x02 is still =x42, please write x7F=x80 and restart from the top)

Write x55=x00 (or other desired g-range)

Write x20=xC0

Write x57=x14

Write x54=x04

Write x56=x08

Write x59=xA0

Write x25=x36

Write x26=x2B

Write x24=xC3

Write xB6=x11

Write xB7=x1E

Write x94=x11

LPF settings (optional):

Write x64=x7E

Write x65=x25

Write x66=xFB

Write x67=x4A

Write x68=x7E

Write x69=x25

Write x6A=x00

Write x6B=x00

Write x6C=xF6

Write x6D=x15

Write x6E=x01

5.6.6 ULTRA LOW NOISE (ULN) SETTINGS

This mode must be used with VDD >=1.8V

This mode is not tested in production and may have offsets and sensitivity errors higher than specified in the tables above.

Write x14=x00 (not necessary if switching from sleep mode)

Delay 10ms (not necessary if switching from sleep mode)

Write x11=x03

Write x14=x03

READ x02 until it's x48 (check for 100 times, if x02 is still =x42, please write x7F=x80 and restart from the top)

Write x55=x00 (or other desired g-range)

Write x20=xC0

Write x57=x1C

Write x54=x06

Write x56=x08

Write x59=xA0

Write x25=x8C

Write x26=x54

Write x24=xC3

Write xB6=x3F

Write xB7=x1E

Write x94=x11

LPF settings (optional):

Write x64=x7E

Write x65=x25

Write x66=xFB

Write x67=x4A

Write x68=x7E

Write x69=x25

Write x6A=x00

Write x6B=x00

Write x6C=xF6

Write x6D=x15

Write x6E=x01

6 INTERFACES

6.1 I2C AND SPI INTERFACES

The device contains both I2C and SPI slave interfaces which share common pins. However, only one interface can be active for correct device operation. The SPI CS pin determines which interface can access the MXC3500AL register. To enable I2C only mode, connect the CS pin to the VDDIO supply.

6.2 I2C INTERFACE

The I2C slave interface operates at a maximum speed of 1 MHz in I2C “Fast Mode Plus”. The SDA (data) is an open-drain, bi-directional pin and the SCL (clock) is an input pin.

The device always operates as an I2C slave or “target”.

An I2C master initiates all communication and data transfers and generates the SCL clock that synchronizes the data transfer. The I2C device address depends upon the settings of various registers and pins as shown in the table below.

7-bit Device ID	8-bit Address (Write)	8-bit Address (Read)	DOUT_A6 level upon power-up
0x4C (0b1001100)	0x98	0x99	GND
0x6C (0b1101100)	0xD8	0xD9	VDDIO

Table 12: I2C Address Selection

The I2C interface remains active if power is applied to the VDDIO and VDD pins. In SLEEP mode the device responds to I2C read and write cycles, but only a limited number of registers are available in the low power state.

Internally, the registers which are used to store samples are clocked by the sample clock and gated by I2C activity. Therefore, to allow the device to collect and present samples in the sample registers at least one I2C STOP condition must be present between samples.

Refer to the I2C specification for a detailed discussion of the protocol. Per I2C requirements, when the I2C interface is enabled, DIN_SDA is an open drain, bi-directional pin. Pins SCK_SCL and DIN_SDA each require an external pull-up resistor, typically 4.7kΩ.

6.2.1 I2C MESSAGE FORMAT

NOTE: At least one I2C STOP condition must be present between samples in order for the device to update the sample data registers.

The device uses the following general format for writing to the internal registers. The I2C master generates a START condition, and then supplies the 7-bit device ID. The 8th bit is the R/W# flag (write cycle = 0). The device pulls DIN_SDA low during the 9th clock cycle indicating a positive ACK.

The second byte is the 8-bit register address of the device to access, and the last byte is the data to write.

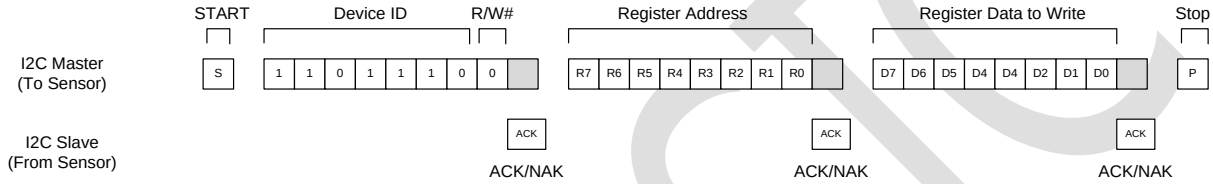


Figure 14: I2C Message Format, Write Cycle, Single Register Write

In a read cycle, the I2C master writes the device ID (R/W#=0) and register address to be read. The master issues a RESTART condition and then writes the device ID with the R/W# flag set to ‘1’. The device shifts out the contents of the register address.

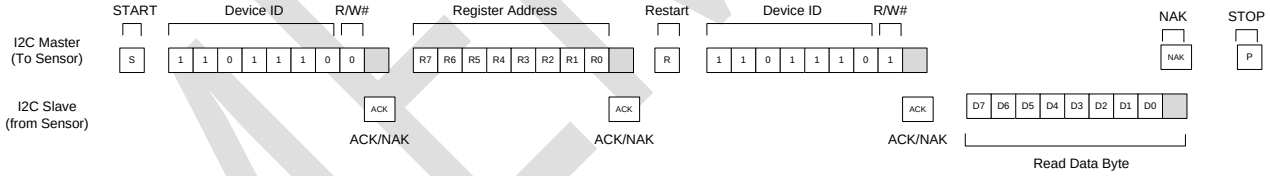


Figure 15: I2C Message Format, Read Cycle, Single Register Read

The I2C master may write or read consecutive register addresses by writing or reading additional bytes after the first access. The device will internally increment the register address.

6.3 SPI INTERFACE

The device always operates as an SPI slave. An SPI master must initiate all communication and data transfers and generate the SCK_SCL clock that synchronizes the data transfer. The CSN pin must be pulled up to VDDIO when the SPI interface is not in use. The SPI interface can operate in 3-wire or 4-wire mode (default). To enable 3-wire mode, connect the SPI DIN pin to the SPI DOUT pin on the PCB.

6.3.1 SPI PROTOCOL

The general protocol for the SPI interface is shown in the figure below. **Each transaction requires a minimum of 24 cycles of the SPI_CLK.** The falling edge of SPI_CS initiates the start of the SPI bus cycle. When the SPI master is writing data to MXC3500AL via the SPI_DIN pin, data may change when the SPI_CLK is low and must be stable on the rising edge. Similarly, output data written from MXC3500AL to the SPI master is shifted out on the SPI_DOUT pin on the falling edge of SPI_CLK and can be latched by the master on the rising edge of SPI_CLK. Serial data in or out of the device is always MSB first.

The register address space is 256 locations, so a total of 8-address bits is required for each SPI bus cycle. The first byte of the transaction is the command/address byte. During clock ‘1’, the R/W# bit is set to ‘0’ for a write cycle or ‘1’ for a read cycle. Clocks 2 to 8 specify the address to be written to or read from. Following clock 8, clocks 9-16 shift in the second address byte where clock 9 is address bit A7. Any clocks following 16 are for write or read data.

When the SPI master is writing data, data may change when the clock is low, and must be stable on the clock rising edge. Similarly, output data written to the SPI master is shifted out on the falling edge of clock and can be latched by the master on the rising edge of the clock. Serial data in or out of the device is always MSB first.

SINGLE REGISTER WRITE

A single register write consists of a 24 (one byte address) clock transaction. As described above, the first bit is set to ‘0’ indicating a register write followed by the register address. The 8th address bit A7 is at bit 9 of the transaction.

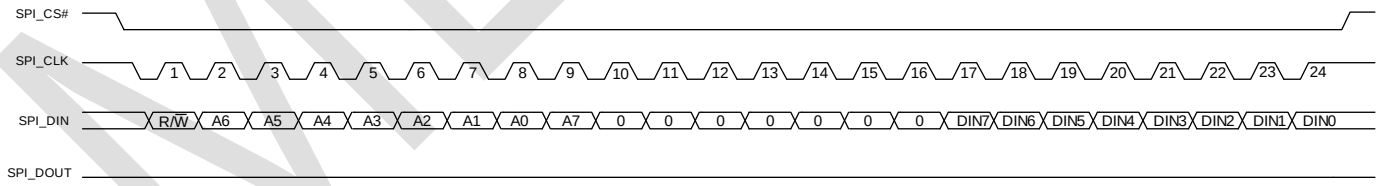


Figure 16: SPI single register write cycle

BURST REGISTER WRITE

A burst or multi-byte register write cycle uses the address specified at the beginning of the transaction as the starting register address. Internally the address will auto-increment to the next consecutive address for each additional byte (8-clocks) of data written beyond clock 24.

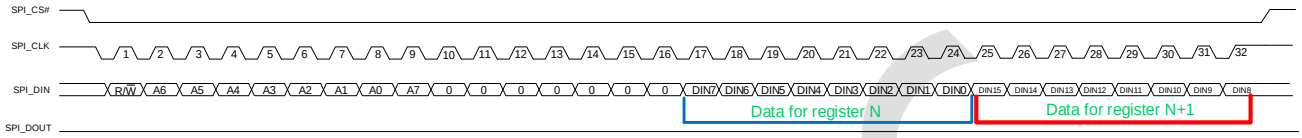


Figure 17: SPI Burst register write cycle (2 registers)

SINGLE REGISTER READ

A single register write consists of a 24 (two-byte address) clock transaction. As described above, the first bit is set to ‘1’ indicating a register write followed by the register address.

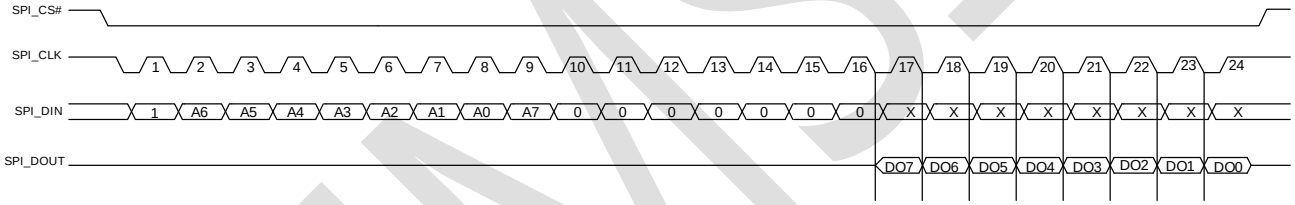


Figure 18: SPI single register read cycle

BURST REGISTER READ

A burst or multi-byte register read cycle uses the address specified at the beginning of the transaction as the starting register address. Internally the address will auto-increment to the next consecutive address for each additional byte (8-clocks) of data read beyond clock 24.

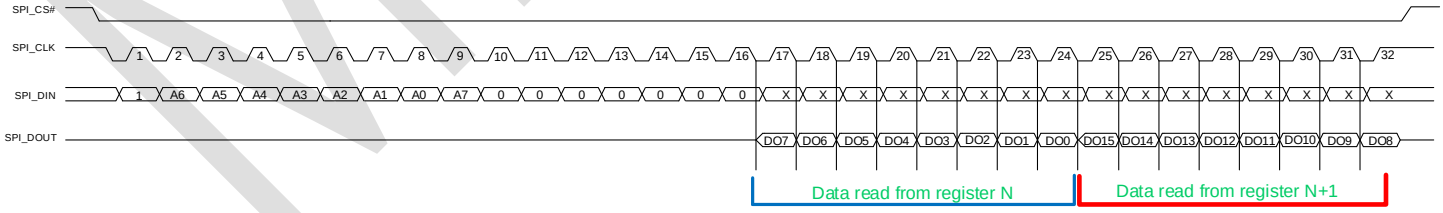


Figure 19: SPI Burst register read cycle (2 registers)

7 REGISTERS

The device has a simple register interface which allows an SPI or I2C master to configure and monitor all aspects of the device. This section lists an overview of user programmable registers. By convention, bit 0 is the least significant bit (LSB) of a byte register.

Note: Do not write to reserved or undefined register addresses or bits.

7.1 SUMMARY

Block	Address (Hex)	Name	Description	Read/ Write	Default (Hex)	Access in SLEEP Mode?
Status Registers						
STATUS	00	**CHIP_ID**	Chip IP Register	RO	F0	Yes
STATUS	01	**VER_ID**	Version ID Register	RO	01	Yes
STATUS	02	**DEV_STATUS_1**	Device Status 1	RO	42	Yes
STATUS	03	**DEV_STATUS_2**	Device Status 2	RO	00	Yes
STATUS	04	**YOUT_LSB**	Y-axis Output, LSB	RO	00	No
STATUS	05	**YOUT_MSB**	Y-axis Output, MSB	RO	00	No
STATUS	06	**XOUT_LSB**	X-axis Output, LSB	RO	00	No
STATUS	07	**XOUT_MSB**	X-axis Output, MSB	RO	00	No
STATUS	08	**ZOUT_LSB**	Z-axis Output, LSB	RO	00	No
STATUS	09	**ZOUT_MSB**	Z-axis Output, MSB	RO	00	No
STATUS	0A	**TEMP_LSB**	Temp Output, LSB	RO	00	No
STATUS	0B	**TEMP_MSB**	Temp Output, MSB	RO	00	No
STATUS	0C-0D	**RESV**	Reserved	RO	00	No
STATUS	0E	**STATUS_REG**	Status Register	R/W	00	No
STATUS	0F	**INTR_STATUS_REG1**	Interrupt Status Register 1	R/W	00	No
STATUS	10	**INTR_STATUS_REG2**	Interrupt Status Register 2	R/W	00	No
SNIFF Registers						
CONTROL	11	**MISC_CTRL_REG**	Miscellaneous Control Register	R/W	20	Yes
CONTROL	12	**SAR_CTRL_REG**	SAR Control Register	R/W	00	Yes
CONTROL	13	**SN1_CTRL_STATUS_REG**	SN1 Control Status Register	R/W	00	Yes
CONTROL	14	**POWER_MODE_CTRL**	Power Mode Control Register	R/W	00	Yes
CONTROL	15	**SNIFF TIMEBASE LSB**	SNIFF Timebase LSB	R/W	00	Yes

Block	Address (Hex)	Name	Description	Read/ Write	Default (Hex)	Access in SLEEP Mode?
CONTROL	16	**SNIFF TIMEBASE MSB**	SNIFF Timebase MSB	R/W	00	Yes
CONTROL	17	**SNIFF_CTRL_REG**	SNIFF Control Register	R/W	00	Yes
CONTROL	18	**SNIFF_BASELINE_Y**	Sniff Baseline Y Register	R/W	00	Yes
CONTROL	19	**SNIFF_BASELINE_X**	Sniff Baseline X Register	R/W	00	Yes
CONTROL	1A	**SNIFF_BASELINE_Z**	Sniff Baseline Z Register	R/W	00	Yes
CONTROL	1B	**SNIFF_TH_Y**	Sniff Threshold Y Register	R/W	00	Yes
CONTROL	1C	**SNIFF_TH_X**	Sniff Threshold X Register	R/W	00	Yes
CONTROL	1D	**SNIFF_TH_Z**	Sniff Threshold Z Register	R/W	00	Yes
CONTROL	1E	**SNIFF_CLOCK_CTRL_REG**	Clock Control Register	R/W	1A	Yes
CONTROL	1F	**SNIFF_IBSEL_CTRL_REG**	IBSEL Control Register	R/W	11	Yes
CONTROL	20	**ADC_CTRL**	ADC Control Register	R/W	00	No
CONTROL	21	**SNIFF_CNT_Y**	SNIFF Count Y Register	R/W	00	No
CONTROL	22	**SNIFF_CNT_X**	SNIFF Count X Register	R/W	00	No
CONTROL	23	**SNIFF_CNT_Z**	SNIFF Count Z Register	R/W	00	No
CONTROL	24	**MODE_CTRL1_REG**	Mode Register (Control Register 1)	R/W	40	No
CONTROL	25	**WAKE TIMEBASE_0**	WAKE Timebase 0	R/W	00	No
CONTROL	26	**WAKE TIMEBASE_1**	WAKE Timebase 1	R/W	00	No
CONTROL	27	**WAKE TIMEBASE_2**	WAKE Timebase 1	R/W	00	No
FIFO Control						
CONTROL	28	**FIFO_CTRL_1_REG**	FIFO Control Register 1	R/W	00	No
CONTROL	29	**FIFO_CTRL_2_REG**	FIFO Control Register 2	R/W	00	No
CONTROL	2A	**FIFO_THRESH_REG**	FIFO Threshold Register	R/W	00	No
Interrupts						
CONTROL	2B	**INTR_CTRL_0**	Interrupt Control Register 0	R/W	00	No
CONTROL	2C	**INTR_CTRL_1**	Interrupt Control Register 1	R/W	00	No
CONTROL	2D	**INTR_CTRL_2**	Interrupt Control Register 2	R/W	00	No
CONTROL	2E	**INT_PAD_CTRL**	INT Pad Control Register	R/W	00	No
CONTROL	2F	**GPIO_CTRL**	GPIO Control Register	R/W	11	No
Motion Registers						
CONTROL	30	**MOTION_CTRL_1**	Motion Control Register 1	R/W	00	No

Block	Address (Hex)	Name	Description	Read/ Write	Default (Hex)	Access in SLEEP Mode?
CONTROL	31	**MOTION_CTRL_2**	Motion Control Register 2	R/W	00	No
CONTROL	32	**TF_THRESH_LSB**	Tilt/Flip Threshold Register LSB	R/W	00	No
CONTROL	33	**TF_THRESH_MSB**	Tilt/Flip Threshold Register MSB	R/W	00	No
CONTROL	34	**TF_DB**	Tilt/Flip Debounce Register	R/W	00	No
CONTROL	35	**AM_THRESH_LSB**	AnyMotion Threshold Register LSB	R/W	00	No
CONTROL	36	**AM_THRESH_MSB**	AnyMotion Threshold Register MSB	R/W	00	No
CONTROL	37	**AM_DB**	AnyMotion Debounce Register	R/W	00	No
CONTROL	38	**SHK_THRESH_LSB**	Shake Threshold Rgister LSB	R/W	00	No
CONTROL	39	**SHK_THRESH_MSB**	Shake Threshold Rgister MSB	R/W	00	No
CONTROL	3A	**PK_P2P_DUR_THRESH_LSB**	Peak P2P Duration Threshold LSB	R/W	00	No
CONTROL	3B	**PK_P2P_DUR_THRESH_MSB**	Peak P2P Duration Threshold MSB	R/W	00	No
CONTROL	3C-3F	**RESV**	Reserved	R/W	00	No
CONTROL	40	**TAP_EVT_THRESH_LSB**	Tap/Dtap Event Threshold LSB	R/W	00	No
CONTROL	41	**TAP_EVT_THRESH_MSB**	Tap/Dtap Event Threshold MSB	R/W	00	No
CONTROL	42	**TAP_SHOCK_DUR**	Tap/Dtap Shock Duration Register	R/W	00	No
CONTROL	43	**TAP_QUIET_DUR**	Tap/Dtap Quiet Duration Register	R/W	00	No
CONTROL	44	**TAP_LATENCY_DUR**	Tap/Dtap Latency Durataion Register	R/W	00	No
CONTROL	45	**TAP_CTRL**	Tap Control Register	R/W	00	No
CONTROL	46	**FREEFALL_THRESH_LSB**	FreeFall Threshold LSB	R/W	00	No
CONTROL	47	**FREEFALL_THRESH_MSB**	FreeFall Threshold MSB	R/W	00	No
CONTROL	48	**FREEFALL_DUR**	FreeFall Duration Register	R/W	00	No
CONTROL	49	**SIXD_HIGH_THRESH_LSB**	SIXD High Threshold LSB	R/W	00	No
CONTROL	4A	**SIXD_HIGH_THRESH_MSB**	SIXD High Threshold MSB	R/W	00	No
CONTROL	4B	**SIXD_LOW_THRESH_LSB**	SIXD Low Threshold LSB	R/W	00	No
CONTROL	4C	**SIXD_LOW_THRESH_MSB**	SIXD Low Threshold MSB	R/W	00	No
STATUS	4D	**SIXD_DUR**	SIXD Duration Register	R/W	00	No
CONTROL	4E	**SIXD_STATUS**	SIXD Status Register	RO	00	No
CONTROL	4F	**RESV**	Reserved	R/W	00	No
CONTROL	50	**INACTIVITY_THRESH_LSB**	Inactivity Threshold LSB	R/W	00	No
CONTROL	51	**INACTIVITY_THRESH_MSB**	Inactivity Threshold MSB	R/W	00	No

Block	Address (Hex)	Name	Description	Read/ Write	Default (Hex)	Access in SLEEP Mode?
CONTROL	52	**INACTIVITY_DUR_LSB**	Inactivity Duration Register LSB	R/W	00	No
CONTROL	53	**INACTIVITY_DUR_MSB**	Inactivity Duration Register MSB	R/W	00	No
CONTROL	54	**WAKE_CTRL_REG**	Wake Control Register	R/W	00	No
CONTROL	55	**RANGE_CTRL**	Range Register	R/W	00	No
CONTROL	56	**DECIMATION_CNT_REG**	Decimation Count Register	R/W	00	No
CONTROL	57	**WAKE_CLOCK_CTRL_REG**	Clock Control Register	R/W	1A	No
CONTROL	58	**RESV**	Reserved	R/W	00	No
CONTROL	59	**WAKE_GCLK_COUNT**	Wake GCLK Burst Count	R/W	A0	No
CONTROL	5A	**TIMESTAMP_B0_LSB**	Timestamp Bank 0 LSB	RO	00	No
CONTROL	5B	**TIMESTAMP_B0_MSB**	Timestamp Bank 0 MSB	RO	00	No
CONTROL	5C	**TIMESTAMP_B1_LSB**	Timestamp Bank 1 LSB	RO	00	No
CONTROL	5D	**TIMESTAMP_B1_MSB**	Timestamp Bank 1 MSB	RO	00	No
CONTROL	5E	**TIMESTAMP_CTRL**	Timestamp Control	R/W	00	No
CONTROL	5F	**RESV**	Reserved	R/W	00	No
FIFO Status						
STATUS	60	**FIFO_STATUS_1**	FIFO Status Register	RO	01	No
STATUS	61	**FIFO_STATUS_2**	FIFO Read Pointer	RO	00	No
STATUS	62	**FIFO_STATUS_3**	FIFO Write Pointer	RO	00	No
STATUS	63	**FIFO_STATUS_4**	FIFO Sample Count	RO	00	No
LPF						
LPF	64	**XL_LPF_B0_L**	XL LPF Coefficient B0 LSB	R/W	00	No
LPF	65	**XL_LPF_B0_H**	XL LPF Coefficient B0 MSB	R/W	00	No
LPF	66	**XL_LPF_B1_L**	XL LPF Coefficient B1 LSB	R/W	00	No
LPF	67	**XL_LPF_B1_H**	XL LPF Coefficient B1 MSB	R/W	00	No
LPF	68	**XL_LPF_B2_L**	XL LPF Coefficient B2 LSB	R/W	00	No
LPF	69	**XL_LPF_B2_H**	XL LPF Coefficient B2 MSB	R/W	00	No
LPF	6A	**XL_LPF_A1_L**	XL LPF Coefficient A1 LSB	R/W	00	No
LPF	6B	**XL_LPF_A1_H**	XL LPF Coefficient A1 MSB	R/W	00	No
LPF	6C	**XL_LPF_A2_L**	XL LPF Coefficient A2 LSB	R/W	00	No
LPF	6D	**XL_LPF_A2_H**	XL LPF Coefficient A2 MSB	R/W	00	No
LPF	6E	**LPF_CTRL**	LPF Control Register	R/W	00	No

Block	Address (Hex)	Name	Description	Read/ Write	Default (Hex)	Access in SLEEP Mode?
NONE	6F-77	**RESV**	Reserved	RO	00	No
CONTROL	78-7E	**RESV**	Reserved	R/W	00	No
CONTROL	7F	**RESET**	Reset Register	R/W	00	Yes
Trim Registers						
TRIM	80	**XL_MN_YOFFL**	XL Main Y-axis Offset LSB	R/W	OTP	Yes
TRIM	81	**XL_MN_YOFFH**	XL Main Y-axis Offset MSB	R/W	OTP	Yes
TRIM	82	**XL_MN_XOFFL**	XL Main X-axis Offset LSB	R/W	OTP	Yes
TRIM	83	**XL_MN_XOFFH**	XL Main X-axis Offset MSB	R/W	OTP	Yes
TRIM	84	**XL_MN_ZOFFL**	XL Main Z-axis Offset LSB	R/W	OTP	Yes
TRIM	85	**XL_MN_ZOFFH**	XL Main Z-axis Offset MSB	R/W	OTP	Yes
TRIM	86	**XL_MN_YGAIN_L**	XL Main Y-axis Gain LSB	R/W	OTP	Yes
TRIM	87	**XL_MN_YGAIN_H**	XL Main Y-axis Gain MSB	R/W	OTP	Yes
TRIM	88	**XL_MN_XGAIN_L**	XL Main X-axis Gain LSB	R/W	OTP	Yes
TRIM	89	**XL_MN_XGAIN_H**	XL Main X-axis Gain MSB	R/W	OTP	Yes
TRIM	8A	**XL_MN_ZGAIN_L**	XL Main Z-axis Gain LSB	R/W	OTP	Yes
TRIM	8B	**XL_MN_ZGAIN_H**	XL Main Z-axis Gain MSB	R/W	OTP	Yes
TRIM	8C	**XL_SN_YOFF**	XL Sniff Y-axis Offset	R/W	OTP	Yes
TRIM	8D	**XL_SN_XOFF**	XL Sniff X-axis Offset	R/W	OTP	Yes
TRIM	8E	**XL_SN_ZOFF**	XL Sniff Z-axis Offset	R/W	OTP	Yes
TRIM	8F	**XL_SN_TOFF**	XL Sniff T-channel Offset	R/W	OTP	Yes
TRIM	90	**XL_SN_YGAIN**	XL Sniff Y-axis Gain	R/W	OTP	Yes
TRIM	91	**XL_SN_XGAIN**	XL Sniff X-axis Gain	R/W	OTP	Yes
TRIM	92	**XL_SN_ZGAIN**	XL Sniff Z-axis Gain	R/W	OTP	Yes
TRIM	93	**XL_SN_TGAIN**	XL Sniff T-channel Gain	R/W	OTP	Yes
TRIM	94	**XL_POLARITY**	XL polarity Register	R/W	OTP	Yes
TRIM	95-9A	**RESV**	Reserved (Factory Trim)	R/W	OTP	Yes
TRIM	9B	**SAR_OFFSET_SHIFT_XL**	SAR OFFSET SHIFT Register	R/W	OTP	Yes
TRIM	9C	**SAR_OFFSET_SHIFT_TEMP**	SAR OFFSET SHIFT Register (TEMP)	R/W	OTP	Yes
TRIM	9D	**RESV**	Reserved (Factory Trim)	R/W	OTP	Yes
TRIM	9E	**VTRIM_REF_REG**	Voltage Reference Trim Register (Factory Trim)	R/W	OTP	Yes

Block	Address (Hex)	Name	Description	Read/ Write	Default (Hex)	Access in SLEEP Mode?
TRIM	9F	**RBIAS_REF_REG**	RBIAS Current Reference Trim Register (Factory Trim)	R/W	OTP	Yes
TRIM	A0	**RESV**	Reserved (Factory Trim)	R/W	OTP	Yes
TRIM	A1	**RESV**	Reserved (Factory Trim)	R/W	OTP	Yes
TRIM	A2	**RESV**	Reserved (Factory Trim)	R/W	OTP	Yes
TRIM	A3	**RESV**	Reserved (Factory Trim)	R/W	OTP	Yes
TRIM	A4-B5	**RESV**	Reserved (Unused Space)	RO	0x00	N/A
TRIM	B6	**WAKE IBSEL Register**	WAKE Mode IBIAS Select Register	R/W	11	Yes
TRIM	B7	**LDO Control Register**	LDO Control Register	R/W	02	Yes
TRIM	B8-BF	**RESV**	Reserved (Factory Trim)	R/W	OTP	Yes
TRIM	C0-FF	**RESV**	Reserved	R/W	0x00	No

Table 13: MXC3500AL register map summary

7.2 REGISTER DESCRIPTIONS

The resister set is accessed by the I2C or SPI interfaces. Note that reserved registers are not listed.

7.2.1 (0X00) - CHIP ID REGISTER

The Chip ID register will always return the value of 0xF0.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
00	Chip ID Register CHIPID_REG	1	1	1	1	0	0	0	0	0xF0	RO

Table 14: Register 0x00 Chip ID Register

7.2.2 (0X01) - VERSION REGISTER

The Version ID register contains the current revision code of MXC3500AL.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
01	Version ID Register VERID_REG	0	0	0	0	0	0	0	1	0x01	RO

Table 15: Register 0x01 Version ID Register

7.2.3 (0X02) – DEVICE STATUS 1 REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
02	Device Status 1 Register DEV_STATUS 1	OTP_EN	BOOT_ DONE	**RESV**	**RESV**	MODE[3]	MODE[2]	MODE[1]	MODE[0]	0x42	RO

The Device Status 1 Register returns the status of the MODE state machine, whether the BOOT sequence is complete, or if the OTP is enabled. When MXC3500AL is power cycled or executes a POR, a value of **0x42** in this register indicates a successful load from OTP, the I2C address has been sampled, and the device is now in SLEEP mode.

The MODE[3:0] bits are updated at the frequency of the HBOSC (SNIFF) or SYS_OSC (WAKE).

Bit	Name	Description
3:0	MODE[3:0]	MODE State Machine status. Use register 0x14 bits 2:0 to set the operation mode of the state machine. The resulting state can be monitored in this register: 0: IDLE 1: BOOT 2: SLEEP (default) 3: WAIT_SN2_PWR_GOOD 4: WAIT_SN2_PGM_DONE 5: SN1 6: SN2 7: WAIT_WAKE_PWR_GOOD 8: WAIT_WAKE_PGM_DONE 9: WAKE A: WAKE_INACTIVITY
5:4	RESV	Reserved
6	BOOT_DONE	0: Boot state machine is in progress. 1: Boot state machine has completed initialization. (default)
7	OTP_EN	0: OTP is not enabled or powered. (default) 1: OTP is enabled or powered.

Table 16: Register 0x02 Device Status Register 1

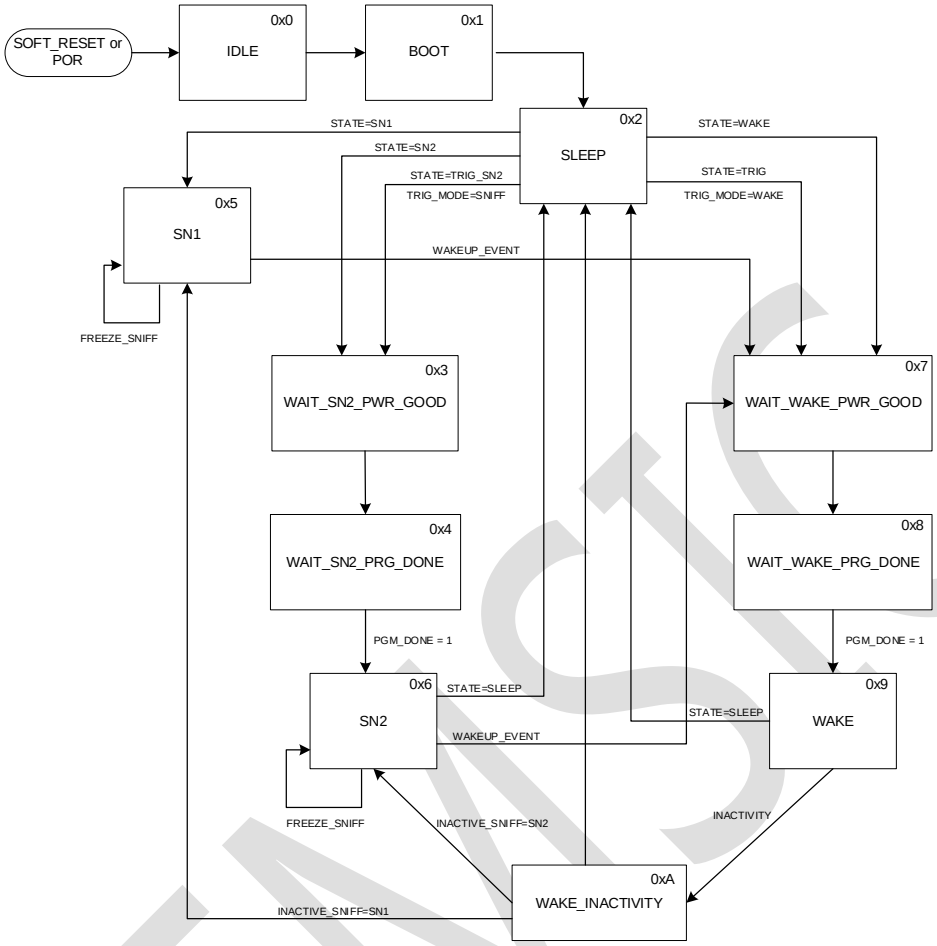


Figure 20: MODE State Machine flow

7.2.4 (0X03) – DEVICE STATUS 2 REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
03	Device Status 2 DEV_STATUS2	**RESV**	**RESV**	**RESV**	**RESV**	OTP_ PWR_ GOOD	FIFO_ PWR_ GOOD	SN2_ PWR_ GOOD	WAKE_ PWR_ GOOD	0x00	RO

This read-only register reports the status of the four switchable power domains.

Bit	Name	Description
0	WAKE_PWR_GOOD	VDD_WAKE power good. 0: VDD WAKE is off 1: VDD WAKE is on
1	SN2_PWR_GOOD	VDD_SN2 (VDD_SNF) power good. 0: VDD_SN2 WAKE is off 1: VDD VDD_SN2 is on
2	FIFO_PWR_GOOD	VDD_FIFO power good. 0: VDD_FIFO WAKE is off 1: VDD_FIFO WAKE is on
3	OTP_PWR_GOOD	OTP_VDD power good. 0: OTP_VDD WAKE is off 1: OTP_VDD WAKE is on This supplies VDD power to the OTP NVM memory.
7:4	RESV	Reserved

Table 17: Device Status register 0x02 bit assignments

7.2.5 (0X04) TO (0X09) – YXZ OUTPUT REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
04	**YOUT_LSB**	XL_YOUT[7]	XL_YOUT[6]	XL_YOUT[5]	XL_YOUT[4]	XL_YOUT[3]	XL_YOUT[2]	XL_YOUT[1]	XL_YOUT[0]	0x00	RO
05	**YOUT_MSB**	XL_YOUT[15]	XL_YOUT[14]	XL_YOUT[13]	XL_YOUT[12]	XL_YOUT[11]	XL_YOUT[10]	XL_YOUT[9]	XL_YOUT[8]	0x00	RO
06	**XOUT_LSB**	XL_XOUT[7]	XL_XOUT[6]	XL_XOUT[5]	XL_XOUT[4]	XL_XOUT[3]	XL_XOUT[2]	XL_XOUT[1]	XL_XOUT[0]	0x00	RO
07	**XOUT_MSB**	XL_XOUT[15]	XL_XOUT[14]	XL_XOUT[13]	XL_XOUT[12]	XL_XOUT[11]	XL_XOUT[10]	XL_XOUT[9]	XL_XOUT[8]	0x00	RO
08	**ZOUT_LSB**	XL_ZOUT[7]	XL_ZOUT[6]	XL_ZOUT[5]	XL_ZOUT[4]	XL_ZOUT[3]	XL_ZOUT[2]	XL_ZOUT[1]	XL_ZOUT[0]	0x00	RO
09	**ZOUT_MSB**	XL_ZOUT[15]	XL_ZOUT[14]	XL_ZOUT[13]	XL_ZOUT[12]	XL_ZOUT[11]	XL_ZOUT[10]	XL_ZOUT[9]	XL_ZOUT[8]	0x00	RO

Table 18: Registers 0x04-0x09 YXZ Output Data

16-BIT OUTPUT DATA

For a read cycle when the FIFO is disabled, registers 0x04 to 0x09 contain the signed output values read from the Y, X, and Z accelerometers. The values are represented as a signed, 2's compliment 16-bit number. Values will range from 0x8000 (full scale negative) to 0x7FFF (full scale positive). The actual output range will be affected by the selected g-range and the analog gain of the SDM.

16-BIT FIFO OUTPUT DATA

For a read cycle when the FIFO is enabled, registers 0x04 to 0x09 contain the YXZ data that is at the output of the FIFO SRAM read bus. A read cycle to address 0x04 will cause the FIFO logic to generate a read strobe to the FIFO, and all 48-bits in registers 0x04 to 0x09 will be updated. Values will range from 0x8000 (full scale negative) to 0x7FFF (full scale positive).

$X^2 + Y^2 + Z^2$ MAGNITUDE DATA

MXC3500AL can compute the magnitude of $X^2 + Y^2 + Z^2$ in hardware. Register 0x54 bit 5 (SQ_OUT) set to '1' outputs this unsigned value in the YOUT and XOUT output registers 0x04 to 0x07.

7.2.6 (0X0A,0X0B) – TEMPERATURE OUTPUT DATA REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0A	**TEMP_LSB**	TEMP_DATA [7]	TEMP_DATA [6]	TEMP_DATA [5]	TEMP_DATA [4]	TEMP_DATA [3]	TEMP_DATA [2]	TEMP_DATA [1]	TEMP_DATA [0]	0x00	RO
0B	**TEMP_MSB**	TEMP_DATA [15]	TEMP_DATA [14]	TEMP_DATA [13]	TEMP_DATA [12]	TEMP_DATA [11]	TEMP_DATA [10]	TEMP_DATA [9]	TEMP_DATA [8]	0x00	RO

Table 19: Register 0x0A/0x0B Temperature Output

The 15-bit temperature sensor data is reported registers 0x0A and 0x0B. The temperature channel is sampled using the XL SDM/ADC and signal path. There is no corresponding interrupt or status bit for the temperature. Temperature scaling and calibration are pending full device characterization.

7.2.7 (0X0E) – STATUS REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0E	Status Register	FLIP_FLAG	TF_FLAG	FIFO_FLAG	RESV	SHAKE_FLAG	ANYM_FLAG	XL_SAMPLE_FLAG	**RESV**	0x00	R/W

Note that bit 2, XL_SAMPLE_FLAG is the only read/write bit in this register.

Bit	Name	Description	R/W
0	RESV	Reserved, not used.	Read only
1	XL_SAMPLE_FLAG	0: No new sample data has arrived since last read. (default) 1: New sample data has arrived and has been written output registers. This bit is set each time the XL acquires a new sample. It is only set upon completion of the Z-channel sample. By writing a '1' to this bit, the flag can be cleared and rearmed to transition for the next sample (e.g., polling). This is the only flag in this register with this feature.	Read/write
2	ANYM_FLAG	0: Any motion condition is not detected. 1: Any motion condition detected.	Read only
3	SHAKE_FLAG	0: SHAKE condition is not detected. 1: SHAKE condition detected.	Read only
4	RESV	Reserved, not used.	Read only
5	FIFO_FLAG	This flag is an OR of the three FIFO flags from register 0x60, FIFO_FULL, FIFO_THRESH, and FIFO_EMPTY.	Read only
6	TILT_FLAG	0: TILT condition is not detected. 1: TILT condition detected.	Read only
7	FLIP_FLAG	0: FLIP condition is not detected. 1: FLIP condition detected.	Read only

Table 20: Status register 0x0E bit assignments

7.2.8 (0X0F) - INTERRUPT STATUS REGISTER 1

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0F	Interrupt Status Register 1	FLIP_INTR	TF_INTR	FIFO_INTR	RESV	SHAKE_INTR	ANYM_INTR	XL_SAMPLE_INTR	**RESV**	0x00	RW

The MXC3500AL sets interrupts in this register. To clear an interrupt, write a bitmask with the bit to clear set to '1' to register 0x0F.

Bit	Name	Description
0	RESV	Reserved, not used.
1	XL_SAMPLE_INTR	0: No new sample data has arrived since last read. 1: New sample data has arrived and has been written output registers.
2	ANYM_INTR	0: Any motion condition is not detected. 1: Any motion condition detected.
3	SHAKE_INTR	0: SHAKE condition is not detected. 1: SHAKE condition detected.
4	RESV	Reserved, not used.
5	FIFO_INTR	This flag is an OR of the three FIFO flags from register 0x0A, FIFO_FULL, FIFO_THRESH, and FIFO_EMPTY.
6	TILT_INTR	0: TILT condition is not detected. 1: TILT condition detected.
7	FLIP_INTR	0: FLIP condition is not detected. 1: FLIP condition detected.

Table 21: Register 0x0F bit assignments

7.2.9 (0X10) - INTERRUPT STATUS REGISTER 2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
10	Interrupt Status Register 2	**RESV**	**RESV**	**RESV**	FREEFALL_ INTR	SIXD_INTR	TTAP_INTR	DTAP_INTR	TAP_INTR	0x00	RW

The MXC3500AL sets interrupts in this register. To clear an interrupt, write a bitmask with the bit to clear set to '1' to register 0x10.

Bit	Name	Description
0	TAP_INTR	0: Tap event/interrupt has not been detected. 1: Tap event/ interrupt has been detected. Write '1' to this bit to clear.
1	DTAP_INTR	0: Double Tap event/interrupt has not been detected. 1: Double Tap event/ interrupt has been detected. Write '1' to this bit to clear.
2	TTAP_INTR	0: Triple Tap event/interrupt has not been detected. 1: Triple Tap event/interrupt has been detected. Write '1' to this bit to clear.
3	SIXD_INTR	0: Change in 6D origination threshold/interrupt not detected. 1: Change in 6D origination threshold/interrupt detected. Write '1' to this bit to clear.
4	FREEFALL_INTR	0: Freefall event/interrupt has not been detected. 1: Freefall event/interrupt has been detected Write '1' to this bit to clear.
5	**RESV**	Reserved, not used.
6	**RESV**	Reserved, not used.
7	**RESV**	Reserved, not used.

Table 22: Register 0x10 bit assignments

7.2.10 (0X11) – MISCELLANEOUS CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
11	MISC Control Register	SAR_CLK_INV_N	WAKEUP_INTR	MODE_TR_CNT[4]	MODE_TR_CNT[3]	MODE_TR_CNT[2]	MODE_TR_CNT[1]	MODE_TR_CNT[0]	WAKEUP_INTR_EN	0x20	RW

Bit	Name	Description
0	WAKEUP_INTR_EN	0: SNIFF to WAKE interrupt is not enabled 1: SNIFF to WAKE interrupt is enabled This bit must be set to a '1' for the WAKEUP interrupt to trigger in bit 6. This interrupt enable is in the "always-on" power domain, so it will remain enabled between SNIFF to WAKE modes.
5:1	MODE_TR_CNT[4:0]	Set the transition time for the MODE state machine between major power modes. This 5-bit count sets the number of delay states to wait (heartbeat oscillator clock periods) between major power mode changes like SNIFF to WAKE. Valid delays are 1 to 31 clocks. Note that this adds overhead to system response times or when MXC3500AL begins sampling. Default value: 16 decimal or 0x10
6	WAKEUP_INTR	Read path: 0: SNIFF to WAKE interrupt has not occurred 1: SNIFF to WAKE interrupt has occurred. When a valid WAKEUP condition has detected by the SNIFF logic, this bit will be set to a '1' by hardware. Note bit 0 must be set to '1' for this interrupt to be enabled.
		Write path: 0: WAKEUP interrupt is not cleared or remains pending (default). 1: WAKEUP interrupt is cleared and rearmed. Writing a '1' to this bit clears and rearms the WAKEUP interrupt. Hardware will clear this bit and the external INT1 pad will transition back to its default state. Note bit 0 must be set to '1' for this interrupt to be enabled.
7	SAR_CLK_INV_N	0: SAR clock is inverted to SAR ADC. (default) 1: SAR clock is not inverted to SAR ADC.

Table 23: Register 0x11 bit assignments

7.2.11 (0X12) – SAR CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
12	SAR Control Register	SAR_ CSAMPLE_ SIZE	SAR_ START_ BIT[2]	SAR_ START_ BIT[1]	SAR_ START_ BIT[0]	SAR_ INV_DATA	EN_STAB_ LVL[1]	EN_STAB_ LVL[0]	SAR_ RES[0]	0x00	RW

This register controls settings for the SAR ADC.

Bit	Name	Description
0	SAR_RES	Set the resolution of the SAR. This bit **must** be set to '1' for the SAR to operate correctly. 1: 8-bit
2:1	EN_STAB_LVLl[1:0]	Stability Level, enable additional current to the analog LDO (ALDO). Please contact Memsic for more information. 00: No extra current selected (default) 01: add 12 nA 10: add 30 nA 11: add 42 nA
3	SAR_INV_DATA	0: SAR data is not inverted (default) 1: SAR data is inverted This bit inverts the data read from the SAR ADC.
6:4	SAR_START_BIT[2:0]	These bits **must** be set to '111' for correct operation.
7	SAR_CSAMPLE_SIZE	0: SAR is set to high sensitivity mode. The range of the SAR is approximately +/-4g, with some variability depending on the MEMS sensitivity. This range is useful for detecting low-g events during sniff modes. (default) 1: SAR is set to full scale conversion range, +/-16g.

Table 24: MXC3500AL 1B Register 0x12 bit assignments

7.2.12(0X13) – SNIFF CONTROL AND STATUS REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
13	SN1 Control/Status Register	SN_ SAMPLE_ FLAG	EXT_CLK_ EN	TIMESTAMP_ RESET	HBOSC_ CLKSEL	INACTIVE_ SN1_SN2N	SN_Z_PD	SN_Y_PD	SN_X_PD	0x00	RW

The SNIFF Control/Status register configures options for SNIFF mode and reports status as SNIFF samples are completed. Note this **does not** report if a sniff sample has passed any threshold or wake-up parameters; it only reports one or more sniff samples have been processed.

Bit 7, SN_SAMPLE_DONE (SN_XYZ_DONE) has different read and write behavior. On reads, this bit is set to '1' when a sniff sample has competed. On writes, software may use this bit to clear the flag and rearm it for the next detection. This bit is not self-clearing.

Bit	Name	Description
0	SN_Y_PD	0: Y-axis is sampled during SNIFF mode (default) 1: Y-axis is not sampled during SNIFF mode
1	SN_X_PD	0: X-axis is sampled during SNIFF mode (default) 1: X-axis is not sampled during SNIFF mode
2	SN_Z_PD	0: Z-axis is sampled during SNIFF mode (default) 1: Z-axis is not sampled during SNIFF mode
3	INACTIVE_SN1_SN2_N	Select which SNIFF mode is used when moving from WAKE mode back to SNIFF during inactivity detection. 0: Go to SN2 SNIFF mode once WAKE inactivity is detected (default) 1: Go to SN1 SNIFF mode once WAKE inactivity is detected.
4	HBOSC_CLKSEL	Select which version of the HB oscillator clock is used, divided or undivided. 0: Use 10 kHz, undivided heartbeat oscillator clock (default). 1: Use programmable, divided version of heartbeat oscillator, 5.0 kHz, 2.5 kHz, or 1.25 kHz selections are available. Use register 0x1E bits 6:5 to select the divided clock frequency.

5	TIMESTAMP_RESET	0: Timestamp module is not reset (default) 1: Timestamp module is reset (level, not edge). The timestamp module is reset by setting and clearing this bit. Software must clear this bit; it is not self-clearing.
6	EXT_CLK_EN	0: External clock drive is disabled (default) 1: External clock drive is enabled, the INT2 pad is the source of the external clock input.
7	SN_SAMPLE_FLAG (SN_YXZZ_DONE)	Read path: 0: SNIFF sample is not completed (default) 1: SNIFF sample is complete. This bit will be set to a '1' by hardware when a SNIFF YXZ sample is complete. Sample data may be read in registers 0xD8, 0xD9, and 0xDA if the WAKE power domain is manually enabled.
	SN_SAMPLE_FLAG_CLR (SN_YXZ_DONE_CLR)	Write path: To clear the SN_SAMPLE_FLAG bit, write 0x80 to register 0x13. Bit 7 of register 0x13 is set by the SNIFF hardware, but cleared by SW. If this bit is not cleared between samples, it will remain at a logic '1'.

Table 25: Register 0x13 bit assignments

7.2.13(0X14) – POWER MODE CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
14	Power Mode Control Register	EXT_TRIG_EN	MAN_PWR_CTRL	EXT_TRIG_POL	SN2_FREEZE	SN1_FREEZE	STATE[2]	STATE[1]	STATE[0]	0x00	RW

Bit	Name	Description
2:0	STATE[2:0]	Set the operational mode of MXC3500AL: 000: Go to SLEEP 001: Go to SN1 010: Go to SN2 011: Go to WAKE 100: Reserved 101: Reserved 110: Reserved 111: Reserved The operation modes SN2 and WAKE will only take place after register programming is complete, and the PGM_DONE bit in register 0x24 bit 7 is set by software. See section 7.2.22 for more information on the PGM_DONE bit.
3	SN1_FREEZE	Keep the mode state machine in the SN1 state. 0: Mode state machine can transition normally. (default) 1: Mode state machine is kept in SN1 state.
4	SN2_FREEZE	Keep the mode state machine in the SN2 state. 0: Mode state machine can transition normally. (default) 1: Mode state machine is kept in SN2 state.
5	EXT_TRIG_POL	External trigger polarity. 0: External trigger is falling edge 1: External trigger is rising edge
6	RESV	Reserved. Must be set to '0'.
7	EXT_TRIG_EN	Enable external trigger operation.

		0: External trigger operation is disabled (default) 1: External trigger mode is enabled.

Table 26: Register 0x14 bit assignments

7.2.14(0X15,0X16) – SNIFF TIMEBASE REGISTERS

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x15	SNIFF_ TIMEB_LSB	Sniff Timebase Register LSB	SN_TB[7]	SN_TB[6]	SN_TB[5]	SN_TB[4]	SN_TB[3]	SN_TB[2]	SN_TB[1]	SN_TB[0]	0x00	R/W
0x16	SNIFF_ TIMEB_ MSB	Sniff Timebase Register MSB	SN_TB[15]	SN_TB[14]	SN_TB[13]	SN_TB[12]	SN_TB[11]	SN_TB[10]	SN_TB[9]	SN_TB[8]	0x00	R/W

Bit	Name	Function	Description
0x15 [7:0] **0x16 [7:0]**	SN_TB[15:0]	Clock count for XL ODR/sample rate generation	The SNIFF timebase registers 0x15 and 0x16 form a 16-bit value that is directly loaded into the output data rate (ODR) generator to allow control over ODR frequency. This is the ODR/sample rate in SNIFF mode. The 16-bit clock count is the number of data_clk periods to wait before executing the start of a new sample for the XL in SNIFF mode. The total number of clock counts to wait must exceed the SAR processing overhead for whatever XL channels are active.

Table 27: Register 0x15/0x16 bit assignments

7.2.15 (0X17) – SNIFF CONTROL REGISTER

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x17	SNIFF_CTRL_REG	Sniff Control Register	DCM_EN	SNIFF_TRIG	SNIFF_TRIG_EN	SNIFF_MODE[1]	SNIFF_MODE[0]	SNIFF_COUNT_EN	SNIFF_AND_OR_MODE	TIME_BASE_EN	0x00	R/W

Bit	Name	Function	Description
0	TIMEBASE_EN	Enable SNIFF timebase/ODR generation	Enables SNIFF Timebase. This bit enables the ODR (output data rate) counter. By default, this counter uses the HB oscillator as a sample clock. To select the system oscillator as the sample clock, use the SN1_SYSCLK_EN bit in register 0x1E bit 7. 0 : SNIFF Timebase Disabled (default) 1 : SNIFF Timebase Enabled
1	SNIFF_AND_OR_MODE	SNIFF Logic Mode	Sets the logical mode for combining of Y/X/Z SNIFF wakeup events before an interrupt is generated. To remove one of the channels (axis) from the equation, use the corresponding axis PD bit in register 0x13 bits [2:0]. “OR” operation is the default. 0: OR - SNIFF wakeup/interrupt is triggered when any of the active channels have met detection threshold and count requirements. (default) 1: AND - SNIFF wakeup/interrupt is triggered when all active. **In SN1 mode only OR mode is supported .**
2	SNIFF_COUNT_EN	SNIFF Count Enable	This bit enables the SNIFF detection counts for all channels. This functionality can be used only in SN2 mode and not in SN1 mode. The detection count logic will increment the count for each event that is above the sniff threshold in registers 0x18, 0x19, and 0x1A. 0: Do not use SNIFF detection counters. (default) 1: Enable SNIFF detection counts, required for valid SNIFF wakeup.
4:3	SNIFF_MODE[1:0]	Sniff Mode Detection/ Comparison Mode	This bit determines how the SNIFF block computes its delta count. 00: C2P Mode (Current to Previous) – The delta count between current and previous samples is a moving window. The SNIFF logic uses the current sample and the immediate previous sample to compute a delta. (default). 01: C2F Mode (Current to First) The delta count is generated

			from subtracting the current sample from the first sample stored when entering SNIFF mode. 10 : C2B Mode (Current to Baseline) The delta count is generated from subtracting the current sample from the baseline value for the channel. 11 : Reserved
5	SNIFF_TRIG_EN	Sniff Mode Trigger Enable	0: Disable SW trigger mode (default) 1: Enable SW trigger mode, use bit 6 to trigger
6	SNIFF_TRIG	Sniff Mode Trigger	0: SW trigger is inactive (default) 1: SW trigger takes one sample in SNIF mode. This bit is used to trigger a single sample acquisition in SNIFF mode. The bit is not self-clearing, so SW much clear the bit and set it to generate a subsequent trigger. Bit 5, the SW_TRIG_EN, must be '1' to keep the SW trigger mode active.
7	RESV	Reserved	Reserved

Table 28: Register 0x17 bit assignments

7.2.16(0X18,0X19,0X1A) – SNIFF YXZ BASELINE REGISTERS

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x18	SN_BASELINE_Y	Sniff Y Base line Value	SN_BASELINE_Y[7]	SN_BASELINE_Y[6]	SN_BASELINE_Y[5]	SN_BASELINE_Y[4]	SN_BASELINE_Y[3]	SN_BASELINE_Y[2]	SN_BASELINE_Y[1]	SN_BASELINE_Y[0]	0x00	R/W
0x19	SN_BASELINE_X	Sniff X Base line Value	SN_BASELINE_X[7]	SN_BASELINE_X[6]	SN_BASELINE_X[5]	SN_BASELINE_X[4]	SN_BASELINE_X[3]	SN_BASELINE_X[2]	SN_BASELINE_X[1]	SN_BASELINE_X[0]	0x00	R/W
0x1A	SN_BASELINE_Z	Sniff Z Base line Value	SN_BASELINE_Z[7]	SN_BASELINE_Z[6]	SN_BASELINE_Z[5]	SN_BASELINE_Z[4]	SN_BASELINE_Z[3]	SN_BASELINE_Z[2]	SN_BASELINE_Z[1]	SN_BASELINE_Z[0]	0x00	R/W

Bit	Name	Function	Description

0x18 7:0	SN_BASELINE_Y	SNIFF Channel Y Baseline Register	This register is used when SNIFF block is configured for BASELINE mode. This unsigned value is subtracted from every subsequent Y-channel sample.
			
			If (CURRENT_Y_SAMPLE – Y_BASELINE > Y_THRESHOLD)
			valid Y-event detected
			else
			no_valid_Y-event

Bit	Name	Function	Description

0x19 7:0	SN_BASELINE_X	SNIFF Channel X Baseline Register	This register is used when SNIFF block is configured for BASELINE mode. This unsigned value is subtracted from every subsequent X-channel sample.
			
			If (CURRENT_X_SAMPLE – X_BASELINE > X_THRESHOLD)
			valid X-event detected
			else
			no_valid_X-event

Bit	Name	Function	Description

0x1A 7:0	SN_BASELINE_Z	SNIFF Channel Z Baseline Register	This register is used when SNIFF block is configured for BASELINE mode. This unsigned value is subtracted from every subsequent Z-channel sample.
			
			If (CURRENT_Z_SAMPLE – Z_BASELINE > Z_THRESHOLD)
			valid Z-event detected
			else
			no_valid_Z-event

Table 29: Registers 0x18/0x19/0x20 bit assignments

7.2.17(0X1B,0X1C,0X1D) – SNIFF YXZ THRESHOLD REGISTERS

The sniff threshold registers set the comparison level to detect a valid sniff condition. These registers are used in SN1 and SN2 sniff modes. Default threshold resolution is 15.6 mg/bit (tentative pending full device characterization).

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x1B	SNIFF_TH_Y	Sniff Y Threshold Value	SNIFF_TH_Y[7]	SNIFF_TH_Y[6]	SNIFF_TH_Y[5]	SNIFF_TH_Y[4]	SNIFF_TH_Y[3]	SNIFF_TH_Y[2]	SNIFF_TH_Y[1]	SNIFF_TH_Y[0]	0x00	R/W
0x1C	SNIFF_TH_X	Sniff X Threshold Value	SNIFF_TH_X[7]	SNIFF_TH_X[6]	SNIFF_TH_X[5]	SNIFF_TH_X[4]	SNIFF_TH_X[3]	SNIFF_TH_X[2]	SNIFF_TH_X[1]	SNIFF_TH_X[0]	0x00	R/W
0x1D	SNIFF_TH_Z	Sniff Z Threshold Value	SNIFF_TH_Z[7]	SNIFF_TH_Z[6]	SNIFF_TH_Z[5]	SNIFF_TH_Z[4]	SNIFF_TH_Z[3]	SNIFF_TH_Z[2]	SNIFF_TH_Z[1]	SNIFF_TH_Z[0]	0x00	R/W

Bit	Name	Function	Description
0x1B 7:0	SNIFF_TH_Y[7:0]	SNIFF Channel X Threshold Register	SNIFF Threshold, X-axis SNIFF_TH_XY7:0], unsigned threshold value 0 to 255 (independent from X and Z thresholds). This value applies to positive and negative g-events.

Bit	Name	Function	Description
0x1C 7:0	SNIFF_TH_X[7:0]	SNIFF Channel X Threshold Register	SNIFF Threshold, X-axis SNIFF_TH_X[7:0], unsigned threshold value 0 to 255 (independent from Y and Z thresholds). This value applies to positive and negative g-events.

Bit	Name	Function	Description
0x1D 7:0	SNIFF_TH_Z[7:0]	SNIFF Channel Z Threshold Register	SNIFF Threshold, Z-axis SNIFF_TH_Z[7:0], unsigned threshold value 0 to 255 (independent from X and Y thresholds). This value applies to positive and negative g-events.

Table 30: Registers 0x1B/0x1C/0x1D bit assignments

7.2.18 (0X1E) – SNIFF CLOCK CONTROL REGISTER

This register determines the clock configuration when in SNIFF modes (SN1 or SN2).

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x1E	SN_CLK_CTRL	Sniff Clock Control Register	SN1_SYSOSC_EN	HB_OSC_CLKDIV[1]	HB_OSC_CLKDIV[0]	SYS_OSC_FOSC[2]	SYS_OSC_FOSC[1]	SYS_OSC_FOSC[0]	SYS_OSC_NDIV[1]	SYS_OSC_NDIV[0]	0x1A	R/W

Bit	Name	Function	Description
1:0	SYS_OSC_NDIV[1:0]	System Oscillator NDIV Select	00: Selected main oscillator frequency is divided by 1 01: Selected main oscillator frequency is divided by 2 10: Selected main oscillator frequency is divided by 4 11: Selected main oscillator frequency is divided by 8 Bits 4:2 are used to select the main oscillator frequency. Bits 1:0 select the above divide by ratios.
4:2	SYS_OSC_FOSC[2:0]	System Oscillator Frequency Select	000: Main oscillator is 100 kHz 001: Main oscillator is 150 kHz 010: Main oscillator is 350 kHz 011: Main oscillator is 650 kHz 100: Main oscillator is 900 kHz 101: Main oscillator is 1.1 MHz 110: Main oscillator is 1.7 MHz 111: Main oscillator is 2.4 MHz
6:5	HB_OSC_CLKDIV[1:0]	Heartbeat Oscillator Clock Divide Select	00: Heartbeat oscillator is 10 kHz 01: Heartbeat oscillator is 5.0 kHz 10: Heartbeat oscillator is 2.5 kHz 11: Heartbeat oscillator is 1.25 kHz The heartbeat oscillator defaults 10 kHz. To enable the alternate divided frequencies instead, set register 0x13 bit 4 (see section 7.2.12).
7	SN1_SYSOSC_EN	SN1 (SNIIFF1) Block System Oscillator Enable	0: SN1 uses heartbeat oscillator as clock (default) 1: SN1 uses main oscillator as clock This bit has multiple uses: • Setting this bit in SLEEP mode will allow the system oscillator to free run. This allows for testing and/or trimming.

			• In SN1 mode, this bit forces the sniff timebase logic (ODR count), mode state machine, and SAR ADC to use the system oscillator as the main clock.

Table 31: Register 0x1E bit assignments

7.2.19 (0X1F) – SNIFF IB SELECT REGISTER

This register determines bias current settings in SNIFF modes (SN1 or SN2). Some settings are tentative pending device characterization. Please contact Memsic for additional information.

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x1F	SN_IBSEL_CTRL	Sniff IBSEL Control Register	CHG_PUMP_EN	HBOSC_PD	IBSEL[5]	IBSEL[4]	IBSEL[3]	IBSEL[2]	IBSEL[1]	IBSEL[0]	0x11	R/W

Bit	Name	Function	Description
5:0	IBSEL[5:0]	Ibias selection for the main oscillator while in SLEEP, SN1 or SN2 states.	0x00: Minimum value, approximately 1nA 0x11: Default value, approximately 17nA 0x3F: Maximum value, approximately 64nA Step size for the IBSEL value is 1nA/LSB.
6	HBOSC_PD	Heartbeat oscillator power down	0: Heartbeat oscillator is active and enabled (default) 1: Heartbeat oscillator is disabled and powered down. Disabling the heartbeat oscillator removes the clock for the mode state machine. This clock **must** be running for MXC3500AL to respond to operational commands in register 0x14.
7	CHG_PUMP_EN	Change pump enable	0: ADC change pump is not enabled (default) 1: ADC charge pump is enabled. The charge pump is used to boost internal analog nodes when the external VDD supply voltage is at 1.2V.

Table 32: Register 0x1F bit assignments

7.2.20 (0X20) – ADC CONTROL REGISTER

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x20	ADC_ CTRL	ADC Control Register	SDM_ AGAIN[1]	SDM_ AGAIN[0]	TEMP_ SENS_EN_ OVERRIDE	**RESV**	SAR_ OFFSET_ MODE	**RESV**	**RESV**	ADC_ MODE	0x00	R/W

Bit	Name	Function	Description
0	ADC_MODE	ADC select	0: Select SDM ADC for sampling (default) 1: Select SAR ADC for sampling (used for SN1 low power sniff and SN2 sniff modes).
1	**RESV**	**Reserved**	**Reserved**
2	**RESV**	**Reserved**	**Reserved**
3	SAR_OFFSET_MODE	SAR offset mode	Select SAR offset mode. SAR offset mode is used to apply an 8-bit offset to the SAR. See sections 7.2.73 and 7.2.74 for more information. 0: SAR offset mode is disabled 1: SAR offset mode is enabled
4	**RESV**	**Reserved**	**Reserved**
5	TEMP_SENS_ EN_OVERRIDE	Enable temperature sensor override.	Setting this bit enables the temp_sense bias current. 0: Temperature sensor override is disabled. (default) 1: Temperature sensor override is enabled.
7:6	SDM_AGAIN[1:0]	SDM analog gain select	Select the analog gain for the SDM (does not apply to SAR). Please contact Memsic for more information. 00: Analog gain is 2x (default) 01: Analog gain is 1x 10: Analog gain is 0.5x 11: Analog gain is 0.25x

Table 33: Register 0x20 bit assignments

7.2.21(0X21,0X22,0X23) – SNIFF YXZ COUNT REGISTERS

These registers are used in SNIFF mode 2 (SN2) only, and are unableabvile SNIFF mode 1 (SN1).

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x21	SNIFF_CNT_Y	Sniff Y Count Value	RESV	RESV	SNIFF_CNT_Y[5]	SNIFF_CNT_Y[4]	SNIFF_CNT_Y[3]	SNIFF_CNT_Y[2]	SNIFF_CNT_Y[1]	SNIFF_CNT_Y[0]	0x00	R/W
0x22	SNIFF_CNT_X	Sniff X Count Value	RESV	RESV	SNIFF_CNT_X[5]	SNIFF_CNT_X[4]	SNIFF_CNT_X[3]	SNIFF_CNT_X[2]	SNIFF_CNT_X[1]	SNIFF_CNT_X[0]	0x00	R/W
0x23	SNIFF_CNT_Z	Sniff Z Count Value	RESV	RESV]	SNIFF_CNT_Z[5]	SNIFF_CNT_Z[4]	SNIFF_CNT_Z[3]	SNIFF_CNT_Z[2]	SNIFF_CNT_Z[1]	SNIFF_CNT_Z[0]	0x00	R/W

Bit	Name	Function	Description
0x21 5:0	SNIFF_CNT_Y[5:0]	SNIFF Channel Y Detection Count	SNIFF Detection Count, Y-aYis SN_COUNT_Y[5:0], unsigned SNIFF event count, 1 to 62 events, independent from other channels. The detection count is COUNT-1 for the desired number of events (for 1 event =1-1 => 0 loaded into register).
0x21 7:6	RESV	Reserved	Reserved

Table 34: Register 0x21 bit assignments

Bit	Name	Function	Description
0x22 5:0	SNIFF_CNT_X[5:0]	SNIFF Channel X Detection Count	SNIFF Detection Count, X-axis SN_COUNT_X[5:0], unsigned SNIFF event count, 1 to 62 events, independent from other channels. The detection count is COUNT-1 for the desired number of events (for 1 event =1-1 => 0 loaded into register).
0x22 7:6	RESV	Reserved	Reserved

Table 35: Register 0x22 bit assignments

Bit	Name	Function	Description
0x23 5:0	SNIFF_CNT_Z[5:0]	SNIFF Channel Z Detection Count	SNIFF Detection Count, Z-axis SN_COUNT_Z[5:0], unsigned SNIFF event count, 1 to 62 events, independent from other channels. The detection count is COUNT-1 for the desired number of events (for 1 event =1-1 => 0 loaded into register).
0x23 7:6	RESV	Reserved	Reserved

Table 36: Register 0x23 bit assignments

7.2.22 (0X24) – MODE CONTROL REGISTER

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x24	MODE_CTRL	MODE Control Register	PGM_DONE	T_PD	Z_PD	Y_PD	X_PD	RESV	WAKE_MODE_2_EN	WAKE_MAN_TIMEBASE_EN	0x40	R/W

Bit	Name	Function	Description
0	WAKE_MAN_TIMEBASE_EN	Enable ODR generation for WAKE mode	0: WAKE and SN2 ODR (output data rate) generation is disabled. 1: WAKE and SN2 ODR generation is enabled. This bit controls rate clock generation for the main pipeline. The ODR determined by the 20-bit count value loaded into registers 0x25-0x27.
1	WAKE_MODE2_EN	Enable 2-filter mode	0: One filter mode, only one filter is used (default) 1: Two filter mode, both filters are used for sampling. This bit determines if one or two filters are used for sampling. This effectively doubles the ODR/sample rate for no change in the system oscillator speed.
2	RESV	Reserved	Reserved
3	Y_PD	Enable/Disable Y-channel sampling for SN2/WAKE mode	0: Y-axis sampling is enabled 1: Y-axis sampling is disabled
4	X_PD	Enable/Disable X-channel sampling for SN2/WAKE mode	0: X-axis sampling is enabled 1: X-axis sampling is disabled
5	Z_PD	Enable/Disable Z-channel sampling for SN2/WAKE mode	0: Z-axis sampling is enabled 1: Z-axis sampling is disabled
6	T_PD	Enable/Disable T-channel sampling for SN2-SAR mode.	0: T-channel sampling is enabled 1: T-channel sampling is disabled (default) Note there is no T-channel sampling using the SDM ADC. All T-channel sampling is performed with the SAR ADC. It is important to make sure this bit is set to a '1' when using the SDM ADC when the contents of register 0x24 are changed.
7	PGM_DONE	Tell the mode state machine register programming is complete for SN2/WAKE mode and that MXC3500AL is ready to start SN2/sniff sampling or WAKE sampling.	0: Software is not done programming SN2 or WAKE mode registers. (default) 1: Software has completed SN2 or WAKE mode programming, and the mode state machine may enter the SN2 or WAKE sampling state.

			The mode state machine monitors this bit to prevent transitioning to an active sampling state like SN2 or WAKE before SW has completed programming all required registers. Although the “SN2” or “WAKE” operational mode can be set in register 0x14, the Power Mode Control register, the final transition into SN2 or WAKE sampling modes is contingent on register 0x24 bit 7, the PGM_DONE bit. Software can determine if the mode state machine is waiting for the PGM_DONE bit to be set by monitoring register 0x02, the Device Status Register 1. **If register 0x02 bits 3:0 is set to 0x4 or 0x8, the state machine is waiting for the PGM_DONE bit to be set in register 0x24 bit 7**. The states of the mode state machine are: x0: IDLE x1: BOOT x2: SLEEP x3: WAIT_SN2_PWR_GOOD **x4: WAIT_SN2_PGM_DONE <= waiting for PGM_DONE** x5: SN1 x6: SN2 x7: WAIT_WAKE_PWR_GOOD **x8: WAIT_WAKE_PGM_DONE <= waiting for PGM_DONE** x9: WAKE xA: WAKE_INACTIVITY

Table 37: Register 0x24 bit assignments

7.2.23(0X25,0X26,0X27) – WAKE TIMEBASE REGISTERS

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x25	WAKE_ TIMEB_0	Wake Timebase Register 0	WK_ TB[7]	WK_ TB[6]	WK_ TB[5]	WK_ TB[4]	WK_ TB[3]	WK_ TB[2]	WK_ TB[1]	WK_ TB[0]	0x00	R/W
0x26	WAKE_ TIMEB_1	Wake Timebase Register 1	WK_TB [15]	WK_TB [14]	WK_TB [13]	WK_TB [12]	WK_TB [11]	WK_TB[10]	WK_TB [9]	WK_TB [8]	0x00	R/W
0x27	WAKE_ TIMEB_2	Wake Timebase Register 2	WK_TB [19]	WK_TB [18]	WK_TB [17]	WK_TB [16]	RESV	RESV	RESV	RESV	0x00	R/W

Bit	Name	Function	Description
0x25 [7:0] 0x26 [7:0] 0x27[7:4]	WK_TB[19:0]	Clock count for XL ODR/sample rate generation, WAKE mode only.	The WAKE timebase registers 0x25,0x26, and 0x27 form a 20-bit value that is directly loaded into the output data rate (ODR) generator to allow control over ODR frequency. This is the ODR/sample rate in WAKE mode. The 20-bit clock count is the number of clock periods to wait before executing the start of a new sample for the XL in WAKE mode. The total number of clocks to wait must exceed the SAR or SDM processing overhead for whatever XL channels are active. Please contact Memsic for more information.

Table 38: Registers 0x25/0x26/0x27 bit assignments

7.2.24 (0X28) – FIFO CONTROL REGISTER 1

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x28	FIFO_ CTRL_1	FIFO Control Register 1	FIFO_ OUTPUT_ EN	FIFO_EN	FIFO_ THRESH_ MODE	FIFO_ RESET	FIFO_ SP_ACC	FIFO_ THRESH_ INTR_EN	FIFO_ FULL_ INTR_EN	FIFO_ THRESH_ PP_ MODE	0x00	R/W

Bit	Name	Function	Description
0	FIFO_THRESH_PP_MODE	Enable FIFO threshold, ping-pong mode	0: FIFO threshold ping-pong mode is disabled (default) 1: FIFO threshold ping-pong mode is enabled. This bit allows the two SRAMs in the FIFO to operate as a ping-pong buffer; while one FIFO SRAM bank is receiving new sample data, the other SRAM can be read by the serial interface/host.
1	FIFO_FULL_INTR_EN	Enable FIFO full interrupt	0: FIFO full interrupt is disabled (default) 1: FIFO full interrupt is enabled.
2	FIFO_THRESH_INTR_EN	Enable FIFO threshold interrupt	0: FIFO threshold interrupt is disabled (default) 1: FIFO threshold interrupt is enabled.
3	FIFO_SP_ACC	FIFO single port access	0: Serial interface cannot read FIFO output in non-PP mode (default) 1: Serial interface can read FIFO output in non-PP mode. If bit 0 is not '1', then the FIFO operates as a write OR read buffer. The FIFO can be accessed by the main pipeline (write data) or the serial interface (read data). This bit is used when the FIFO is not operating in ping-pong mode.
4	FIFO_RESET	FIFO reset	0: FIFO logic is not reset (default) 1: FIFO logic is reset. This is a local reset to the FIFO logic. It is recommended to always reset the FIFO when first powering up the FIFO logic.
5	FIFO_THRESH_MODE	FIFO threshold mode enable	0: FIFO threshold mode is disabled (default) 1: FIFO threshold mode is enabled. This bit enables "threshold mode", where the contents of register 0x2A, FIFO Threshold Register, set the level of the FIFO threshold value. Once the amount of data has reached the level of register 0x2A, the FIFO will stop accepting new data.
6	FIFO_EN	FIFO enable	0: FIFO is not enabled (default) 1: FIFO is enabled This bit is the "master enable" for the FIFO logic. This bit must be enabled for any FIFO operation.
7	FIFO_OUTPUT_EN	FIFO output enable	0: FIFO does not drive output registers (default) 1: FIFO does drive output registers 0x04 to 0x09.

Table 39: Register 0x28 bit assignments

7.2.25 (0X29) – FIFO CONTROL REGISTER 2

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x29	FIFO_CTRL_2	FIFO Control Register 2	**RESV**	**RESV**	**RESV**	**RESV**	FIFO_ EMPTY_ INTR_EN	FIFO_ BURST_ MODE	FIFO_ TEST_ MODE	FIFO_ STREAM_ MODE	0x00	R/W

Bit	Name	Function	Description
0	FIFO_STREAM_MODE	Enable FIFO stream mode	0: FIFO stream mode is disabled 1: FIFO stream mode is enabled. FIFO stream mode allows new data to overwrite the oldest data in the FIFO buffer. This acts like one 256-sample rolling buffer, where previous samples can be overwritten until stopped. It always read out the last (latest) 256 samples.
1	RESV	Reserved	Reserved
2	FIFO_BURST_MODE	Enable FIFO burst mode	0: FIFO burst mode is disabled (default) 1: FIFO burst mode is enabled This bit is used to enable FIFO burst mode. Burst mode is defined as '**when the serial interface is going to read out more than one YXZ dataset from the FIFO in the same transaction.'** Reading a single YXZ dataset (one sample) from the FIFO, and then ending the serial read transaction, does not require this bit to be set.
3	FIFO_EMPTY_INTR_EN	FIFO single port access	0: FIFO empty interrupt is disabled (default) 1: FIFO empty interrupt is enabled.
7:4	RESV	Reserved	Reserved

Table 40: Register 0x29 bit assignments

7.2.26 (0X2A) – FIFO THRESHOLD REGISTER

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x2A	FIFO_ THRESH_ REG	FIFO Threshold Register	FIFO_ THRESH[7]	FIFO_ THRESH[6]	FIFO_ THRESH[5]	FIFO_ THRESH[4]	FIFO_ THRESH[3]	FIFO_ THRESH[2]	FIFO_ THRESH[1]	FIFO_ THRESH[0]	0x00	R/W

Bit	Name	Function	Description
7:0	FIFO_THRESHOLD	Set FIFO threshold.	**Non-ping-pong mode** This value sets the number of samples the FIFO will accept before ending data capture. This value can be up to 0xFF (256) for the full size of the FIFO (both SRAM banks combined). See register 0x28 bit 3, FIFO_SP_ACC, FIFO single port access mode. **Ping-Pong Mode** This value sets the "virtual bank size" of the FIFO. Each SRAM in the FIFO can store up to 128 samples each. In ping-pong mode this threshold value must be 128 samples or less. Once the active bank reaches the threshold amount, the FIFO logic stops writing to the current bank, and activates the other bank.

Table 41: Register 0x2A bit assignments

7.2.27(0X2B) – INTERRUPT CONTROL REGISTER 0

This register selects which interrupt(s) are connected to the external INT1 and INT2 pads.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
2B	Interrupt Control Register 0	INT2_SEL[3]	INT2_SEL[2]	INT2_SEL[1]	INT2_SEL[0]	INT1_SEL[3]	INT1_SEL[2]	INT1_SEL[1]	INT1_SEL[0]	0x00	R/W

Bit	Name	Description
3:0	INT1_SEL[3:0]	Select which interrupt drives the INT1 pad. 0: Default (XL interrupt on sample and Motion) 1: XL interrupt on sample 2: Shake 3: AnyMotion 4: Flip 5: Tilt 6: Reserved 7: Tap 8: Double Tap 9: Triple Tap A: Freefall B: Six 6D Orientation C: FIFO Interrupt D: INT1_INT2 Combined Interrupt E: Reserved F: Reserved
7:4	INT2_SEL[3:0]	Select which interrupt drives the INT2 pad. 0: Default (FIFO interrupts) 1: XL interrupt on sample 2: Shake 3: AnyMotion 4: Flip 5: Tilt 6: Reserved 7: Tap 8: Double Tap 9: Triple Tap A: Freefall

		B: Six 6D Orientation C: FIFO Interrupt D: INT1_INT2 Combined Interrupt E: Reserved F: Reserved

Table 42: Register 0x2B bit assignments

7.2.28 (0X2C) – INTERRUPT CONTROL REGISTER 1

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
2C	Interrupt Control Register 1	FLIP_ INT_EN	TILT_ INT_EN	FIFO_ INT_EN	RESV	SHAKE_ INT_EN	ANYM_ INT_EN	ACQ_XL_ INT_EN	RESV	0x00	R/W

Note that the corresponding motion feature must be enabled in registers 0x30 or 0x31 must be enabled for the interrupt to actual transition. The corresponding FIFO interrupt must be enabled in registers 0x28 or 0x29.

Bit	Name	Description
0	RESV	Reserved, not used.
1	ACQ_XL_INT_EN	0: XL interrupt is disabled (default) 1: XL interrupt is enabled.
2	ANYM_INT_EN	0: AnyMotion interrupt is disabled (default) 1: AnyMotion interrupt is enabled.
3	SHAKE_INT_EN	0: Shake interrupt is disabled (default) 1: Shake interrupt is enabled.
4	RESV	Reserved, not used.
5	FIFO_INT_EN	0: FIFO interrupt is disabled (default) 1: FIFO interrupt is enabled.
6	TILT_INT_EN	0: TILT interrupt is disabled (default) 1: TILT interrupt is enabled.
7	FLIP_INT_EN	0: FLIP interrupt is disabled (default) 1: FLIP interrupt is enabled.

Table 43: Register 0x2C bit assignments

7.2.29 (0X2D) – INTERRUPT CONTROL REGISTER 2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
2D	Interrupt Control Register 2	**RESV**	**RESV**	**RESV**	FREEFALL_ INTR_EN	SIXD_ INTR_EN	TTAP_ INTR_EN	DTAP_ INTR_EN	TAP_ INTR_EN	0x00	R/W

Note that the corresponding motion feature must be enabled in registers 0x30 or 0x31 must be enabled for the interrupt to actual transition.

Bit	Name	Description
0	TAP_INTR_EN	0: TAP interrupt is disabled (default) 1: TAP interrupt is enabled.
1	DTAP_INTR_EN	0: DTAP interrupt is disabled (default) 1: DTAP interrupt is enabled.
2	TTAP_INTR_EN	0: TTAP interrupt is disabled (default) 1: TTAP interrupt is enabled.
3	SIXD_INTR_EN	0: SIXD (6D) interrupt is disabled (default) 1: SIXD (6D) interrupt is enabled.
4	FREEFALL INT_EN	0: FREEFALL interrupt is disabled (default) 1: FREEFALL interrupt is enabled.
5	Reserved	Reserved
6	Reserved	Reserved
7	Reserved	Reserved

Table 44: Register 0x2D bit assignments

7.2.30 (0X2E) – INT PAD CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
2E	INT Pad Control Register	SW_TRIG	SW_TRIG_EN	RESV	RESV	INT2_PAD _CFG[1]	INT2_PAD_CFG[0]	INT1_PAD_CFG[1]	INT1_PAD_CFG[0]	0x00	R/W

Bit	Name	Function	Description
1:0	INT1_PAD_CFG[1:0]	INT1 pad configuration control.	00: INT1 pad operates in interrupt request mode as an output (default). 01: INT1 pad operates in external trigger mode as an input. 10: INT1 pad operates in GPIO mode as a general purpose I/O. 11: INT1 pad operates as a test output.
3:2	INT2_PAD_CFG[1:0]	INT2 pad configuration control.	00: INT2 pad operates in interrupt request mode as an output (default). 01: INT2 pad operates in external trigger mode as an input. 10: INT2 pad operates in GPIO mode as a general purpose I/O. 11: INT2 pad operates as a test output.
4	RESV	Reserved	Reserved.
5	RESV	Reserved	Reserved.
6	SW_TRIG_EN	Enable SW trigger mode.	0: SW trigger mode is disabled (default). 1: SW trigger mode is enabled. Use bit 7 to generate trigger.
7	SW_TRIG	Generate a SW trigger.	0: No SW trigger is generated (default). 1: SW trigger is generated. This bit is used to trigger a single sample acquisition. The bit is not self-clearing, so SW much clear the bit and set it to generate a subsequent trigger. Bit 6, the SW_TRIG_EN, must be '1' to keep the SW trigger mode active.

Table 45: Register 0x2E bit assignments

7.2.31 (0X2F) – GPIO CONTROL REGISTER

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x2F	GPIO_CTRL	GPIO Control Register	GPIO2_ INT2_IPP	GPIO2_ INT2_IAH	GPIO2_ OUT_IN_N	GPIO2_ DATA	GPIO1_ INT1_IPP	GPIO1_ INT1_IAH	GPIO1_ OUT_IN_N	GPIO1_ DATA	0x11	R/W

This register is used to select the INT1 pad and INT2 pad polarity and drive mode when the pads are used as interrupt request outputs, or GPIO outputs.

To use the GPIO functionality for the INT1 pad or the INT2 pad, the INT1_PAD_CFG[1:0] or INT2_PAD_CFG[1:0] control bits in register 0x2E must be set to '10'. The options in this register require GPIO mode to be enabled for the corresponding pad.

Bit	Name	Function	Description
0	GPIO1_DATA	GPIO1 input (read) or output path (write)	Read path, configured as an input (bit 1 = 0) 0: INT1 pad input is at 0. 1: INT1 pad input is at 1. Write path, configured as an output (bit 1 = 1) 0: INT1 pad is driven to a logic 0. 1: INT1 pad is driven to a logic 1. In a read cycle, this bit is used to read the state of the INT1 pad. If the pad is configured as an input, then it returns the current level as read from the pad. If the pad is configured as an output, then this bit is the drive level applied to the pad. In a write cycle, this bit is used to set the state of the pad. If the pad is configured as an output, then this bit determines the drive level applied to the pad.
1	GPIO1_OUT_IN_N	Set the direction of INT1 pad (input or output)	0: INT1 pad is configured as an input (default). 1: INT1 pad is configured as an output.
2	GPIO1_INT1_IAH	Set polarity of INT1 output.	0: The INT1 pad is active low. 1: The INT1 pad is active high. This bit sets the polarity level of the INT1 pad. This bit is used in interrupt mode to set the level of the interrupt request, or in GPIO mode to set the level of the GPIO output drive.
3	GPIO1_INT1_IPP	Select open drain or push/pull mode for INT1.	0: The INT1 pad operates in open-drain mode as an output. 1: The INT1 pad operates in push-pull mode as an output. This bit sets the drive mode of the INT1 pad as an interrupt request output, or a GPIO output.
4	GPIO2_DATA	INT2 input (read) or output path (write)	Read path, configured as an input (bit 1 = 0) 0: INT2 pad input is at 0. 1: INT2 pad input is at 1.

			Write path, configured as an output (bit 1 = 1) 0: INT2 pad is driven to a logic 0. 1: INT2 pad is driven to a logic 1. In a read cycle, this bit is used to read the state of the INT2 pad. If the pad is configured as an input, then it returns the current level as read from the pad. If the pad is configured as an output, then this bit is the drive level applied to the pad. In a write cycle, this bit is used to set the state of the pad. If the pad is configured as an output, then this bit determines the drive level applied to the pad.
5	GPIO2_OUT_IN_N	Set the direction of INT2 pad (input or output)	0: INT2 pad is configured as an input (default). 1: INT2 pad is configured as an output.
6	GPIO2_INT2_IAH	Set polarity of INT2 output.	0: The INT2 pad is active low. 1: The INT2 pad is active high. This bit sets the polarity level of the INT2 pad. This bit is used in interrupt mode to set the level of the interrupt request, or in GPIO mode to set the level of the GPIO output drive.
7	GPIO2_INT2_IPP	Select open drain or push/pull mode for INT2.	0: The INT2 pad operates in open-drain mode as an output. 1: The INT2 pad operates in push-pull mode as an output. This bit sets the drive mode of the INT2 pad as an interrupt request output, or a GPIO output.

Table 46: Register 0x2F bit assignments

7.2.32 (0X30) – MOTION CONTROL REGISTER 1

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x30	**MOTION_ CTRL_1**	Motion Control Register 1	**RESV**	TF_ENABLE	SIXD_EN	RESV	SHAKE_EN	ANYM_EN	FREEFALL_EN	TAP_DTAP_EN	0x00	R/W

Bit	Name	Description
0	TAP_DTAP_EN	0: TAP/DTAP/TTAP detection is disabled (default). 1: TAP/DTAP/TTAP detection is enabled.
1	FREEFALL_EN	0: FREEFALL_EN detection is disabled (default). 1: FREEFALL_EN detection is enabled.
2	ANYM_EN	0: Any Motion detection is disabled (default). 1: Any Motion detection is enabled.
3	SHAKE_EN	0: Shake detection is disabled (default). 1: Shake detection is enabled.
4	RESV	Reserved
5	SIXD_EN	0: SIXD (6D) detection is disabled (default). 1: SIXD (6D) detection is enabled.
6	TF_ENABLE	0: Tilt/Flip detection is disabled (default). 1: Tilt/Flip detection is enabled.
7	RESV	Reserved

Table 47: Register 0x30 bit assignments

7.2.33 (0X31) – MOTION CONTROL REGISTER 2

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x31	**MOTION_ CTRL_2**	Motion Control Register 2	MOTION_ RESET	RESV	RESV	RESV	AUTO_ CLR_EN	RAW_ PROC_STAT	Z_AXIS_ORT	MOTION_ LATCH	0x00	R/W

Bit	Name	Description
0	MOTION_LATCH	0: Motion block does not latch outputs (default) 1: Motion block latches outputs This bit is generally not used if motion interrupts are enabled. The interrupt latch and auto-clear feature in bit 3 is the preferred configuration.
1	Z_AXIS_ORT	0: Z-axis orientation is positive through top of package. (default) 1: Z-axis orientation is positive through bottom of package. The Z-axis orientation (Motion Control Register 0x31 bit 1) tells the logic which way the packaged device is mounted. A value of '0' is used for a bottom mount, and '1' is used for a top mount. Note, this bit does not affect the polarity setting of the Z-axis, only with respect to the motion detection algorithms.
2	RAW_ PROC_STAT	0: Motion flag bits are filtered by debounce and other settings (default) 1: Motion flag bits provide real-time, raw motion information, useful for debug.
3	AUTO_ CLR_EN	0: SIXD (6D) interrupt is disabled (default) 1: SIXD (6D) interrupt is enabled.
5:4	RESV	Reserved
6	RESV	Reserved
7	MOTION_ RESET	0: Motion block is not in reset (default) 1: The motion block is held in reset. SW must clear this bit for the reset to be released. This bit is not self-clearing.

Table 48: Register 0x31 bit assignments

7.2.34 (0X32,0X33) – TILT/FLIP THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x32	Tilt/Flip Threshold Register LSB	TF_THR[7]	TF_THR[6]	TF_THR[5]	TF_THR[4]	TF_THR[3]	TF_THR[2]	TF_THR[1]	TF_THR[0]	0x00	R/W
0x33	Tilt/Flip Threshold Register MSB	RESV	TF_THR[14]	TF_THR[13]	TF_THR[12]	TF_THR[11]	TF_THR[10]	TF_THR[9]	TF_THR[8]	0x00	R/W

This register is used for both the Flat/Tilt/Flip algorithms.

For Flat/Tilt/Flip algorithm, this register holds the programmed 15-bit threshold value to detect Flat/Tilt/Flip position of the device. If the sample value is greater than the programmed value of this register, then a Tilt condition is detected. If the sample value is less than the programmed value of this register, then a Flat/Flip condition is detected depending on the sample value of the z-axis and by the way the chip is mounted on the platform which is determined by z-axis-orient bit which is Reg. 0x31 bit 1.

The threshold value is in terms of digital gain stage of the pipeline, prior to any range g-scale. For a 1.4fF/g sensitivity MEMS, this corresponds to a signed 15-bit, +/-24g reference frame of digital offset and gain corrected data (tentative, pending device characterization).

7.2.35(0X34) – TILT/FLIP DEBOUNCE REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x34	Tilt/Flip Debounce Register	TF_DB[7]	TF_DB[6]	TF_DB[5]	TF_DB[4]	TF_DB[3]	TF_DB[2]	TF_DB[1]	TF_DB[0]	0x00	R/W

This register holds the programmed debounce value to detect the Tilt/Flip condition and set the corresponding interrupt. Once a Tilt/Flip condition is detected for the duration programmed in this register, the Tilt/Flip interrupt is set in the interrupt register. The debounce count is in terms of consecutive samples, which increment at the selected output data rate (ODR).

7.2.36(0X35,0X36) – ANYMOTION THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x35	AnyMotion Threshold Register LSB	ANYM_ THR[7]	ANYM_ THR[6]	ANYM_ THR[5]	ANYM_ THR[4]	ANYM_ THR[3]	ANYM_ THR[2]	ANYM_ THR[1]	ANYM_ THR[0]	0x00	R/W
0x36	AnyMotion Threshold Register MSB	RESV	ANYM_ THR[14]	ANYM_ THR[13]	ANYM_ THR[12]	ANYM_ THR[11]	ANYM_ THR[10]	ANYM_ THR[9]	ANYM_ THR[8]	0x00	R/W

This register holds the programmed 15-bit threshold value to detect Any_Motion. If, the delta of the current sample value and the previous sample value, is greater than the programmed value of this register, then Any_Motion condition is detected.

The threshold value is in terms of digital gain stage of the pipeline, prior to any range g-scale. For a 1.4fF/g sensitivity MEMS, this corresponds to a signed 15-bit, +/-24g reference frame of digital offset and gain corrected data (tentative, pending device characterization).

7.2.37(0X37) – ANYMOTION DEBOUNCE REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x37	AnyMotion Debounce Register	ANYM_DB [7]	ANYM_DB [6]	ANYM_DB [5]	ANYM_DB [4]	ANYM_DB [3]	ANYM_ DB[2]	ANYM_ DB[1]	ANYM_ DB[0]	0x00	R/W

Once an Any_Motion condition is detected, the Any_Motion interrupt is set in the interrupt register. This register holds the programmed debounce value to clear the Any_Motion interrupt set in the interrupt register.

For the duration programmed in this register, if the Any_Motion condition is not detected, then the Any_Motion interrupt is cleared in the interrupt register. The debounce count is in terms of consecutive samples, which increment at the selected output data rate (ODR).

7.2.38(0X38,0X39) – SHAKE THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x38	**Shake Threshold Register LSB**	SH_THR[7]	SH_THR[6]	SH_THR[5]	SH_THR[4]	SH_THR[3]	SH_THR[2]	SH_THR[1]	SH_THR[0]	0x00	R/W
0x39	**Shake Threshold Register MSB**	SH_ THR[15]	SH_ THR[14]	SH_ THR[13]	SH_ THR[12]	SH_ THR[11]	SH_THR[10]	SH_THR[9]	SH_THR[8]	0x00	R/W

This register holds the programmed 15-bit threshold value to detect Shake. If, the delta of the current sample value and the previous sample value, is greater than +/- programmed value of this register, then Shake condition is detected.

The threshold value is in terms of digital gain stage of the pipeline, prior to any range g-scale. For a 1.4fF/g sensitivity MEMS, this corresponds to a signed 15-bit, +/-24g reference frame of digital offset and gain corrected data (tentative, pending device characterization).

7.2.39(0X3A,0X3B) – SHAKE PEAK 2 PEAK DURATION THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x3A	Peak P2P Duration Threshold LSB	PK_P2P_DUR[7]	PK_P2P_DUR[6]	PK_P2P_DUR[5]	PK_P2P_DUR[4]	PK_P2P_DUR[3]	PK_P2P_DUR[2]	PK_P2P_DUR[1]	PK_P2P_DUR[0]	0x00	R/W
0x3B	Peak P2P Duration Threshold MSB	RESV	SHK_CNT_DUR[2]	SHK_CNT_DUR[1]	SHK_CNT_DUR[0]	PK_P2P_DUR[11]	PK_P2P_DUR[10]	PK_P2P_DUR[9]	PK_P2P_DUR[8]	0x00	R/W

PEAK AND PEAK_TO_PEAK DURATION

This register i.e. 0x3A and 0x3B[3:0] holds the programmed value to detect the Peak and the Peak to Peak width of the Shake.

If the sample value is beyond (+/-) the shake threshold, then a Peak is detected and its width is measured as defined in this register.

If the sample value is within (+/-) the shake threshold, then a Peak to Peak is detected and its width is measured as defined in this register.

The duration count is in terms of consecutive samples, which increment at the selected output data rate (ODR).

SHAKE COUNTER

This register i.e. 0x3B[6:4] holds the programmed value of the number of shake cycles to be detect. Once the programmed number of shake cycles are detected, the Shake interrupt is set in the interrupt status register. The shake count is in terms of consecutive samples, which increment at the selected output data rate (ODR).

7.2.40(0X40,0X41) – TAP EVENT THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x40	TAP/DTAP/TTAP Event Threshold LSB Register	TAP_EVT_TH[7]	TAP_EVT_TH[6]	TAP_EVT_TH[5]	TAP_EVT_TH[4]	TAP_EVT_TH[3]	TAP_EVT_TH[2]	TAP_EVT_TH[1]	TAP_EVT_TH[0]	0x00	R/W
0x41	TAP/DTAP/TTAP Event Threshold MSB Register	**RESV**	TAP_EVT_TH[14]	TAP_EVT_TH[13]	TAP_EVT_TH[12]	TAP_EVT_TH[11]	TAP_EVT_TH[10]	TAP_EVT_TH[9]	TAP_EVT_TH[8]	0x00	R/W

This unsigned threshold value applies to all tap events (single, double, and triple tap). The threshold value is in terms of digital gain stage of the pipeline, prior to any range g-scale. For a 1.4fF/g sensitivity MEMS, this corresponds to a signed 15-bit, +/-24g reference frame of digital offset and gain corrected data (tentative, pending device characterization).

Bit	Name	Function	Description
0x40 7:0 **0x41 6:0**	TAP_EVT_TH[14:0]	Tap Threshold Register	Specifies the threshold above which a tap event is detected. The value is a magnitude and is unsigned.

Table 49: Register 0x40/41 bit assignments

7.2.41(0X42) – TAP SHOCK DURATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x42	TAP/DTAP/TTAP Shock Duration Register	TAP_SHOCK_DUR[7]	TAP_SHOCK_DUR[6]	TAP_SHOCK_DUR[5]	TAP_SHOCK_DUR[4]	TAP_SHOCK_DUR[3]	TAP_SHOCK_DUR[2]	TAP_SHOCK_DUR[1]	TAP_SHOCK_DUR[0]	0x00	R/W

Bit	Name	Function	Description
7:0	TAP_SHOCK_DUR[7:0]	Shock Duration Count for TAP/DTAP/TTAP	Specifies the shock duration in which the acceleration value should come below the tap event detection value . If the acceleration value does not fall below the event detection threshold in this period, then the event is not detected. The count is in terms of ODR/sample periods.

Table 50: Register 0x42 bit assignments

7.2.42(0X43) – TAP QUIET DURATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x43	TAP/DTAP/TTAP Quiet Duration Register	TAP_QUIET_DUR[7]	TAP_QUIET_DUR[6]	TAP_QUIET_DUR[5]	TAP_QUIET_DUR[4]	TAP_QUIET_DUR[3]	TAP_QUIET_DUR[2]	TAP_QUIET_DUR[1]	TAP_QUIET_DUR[0]	0x00	R/W

Bit	Name	Function	Description
7:0	TAP_ QUIET _DUR[7:0]	TAP/DTAP/TTAP Quiet Duration Register	After the shock period there should be no acceleration event above the detection threshold in Quiet Period. If there is an event above the threshold in Quiet Duration, then the tap event is not detected . This value is in terms of ODR or sample periods.

Table 51: Register 0x43 bit assignments

7.2.43(0X44) – TAP LATENCY DURATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x44	TAP Latency Duration Register LSB	TAP_LATENCY_DUR[7]	TAP_LATENCY_DUR[6]	TAP_LATENCY_DUR[5]	TAP_LATENCY_DUR[4]	TAP_LATENCY_DUR[3]	TAP_LATENCY_DUR[2]	TAP_LATENCY_DUR[1]	TAP_LATENCY_DUR[0]	0x00	R/W

Bit	Name	Function	Description
7:0	TAP_LATENCY_DUR[7:0]	Lower 8-bits of the Tap Latency Duration. The upper 5-bits are in register 0x45	Specifies the max delay between 2 successive tap events in generation of double tap and triple tap. This period starts after the quiet period is over the previous event. This value is in terms of ODR or sample periods.

Table 52: Register 0x44 bit assignments

7.2.44(0X45) – TAP CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x45	Tap Control/TAP Latency Duration Register MSB	MASK_Z	MASK_X	MASK_Y	TAP_ LATENCY _DUR[12]	TAP_ LATENCY _DUR[11]	TAP_ LATENCY_ DUR[10]	TAP_ LATENCY_ DUR[9]	TAP_ LATENCY_ DUR[8]	0x00	R/W

Bit	Name	Function	Description
4:0	TAP_LATENCY_DUR[12:8]	Upper 5-bits of the Tap Latency Duration. The lower 8-bits are in register 0x44	Specifies the max delay between 2 successive tap events in generation of double tap and triple tap. This period starts after the quiet period is over the previous event. This value is in terms of ODR or sample periods.
5	MASK_X	Enable/Disable Y-channel tap event detection	0: Y channel tap detection enabled (default) 1: Y channel tap detection disabled
6	MASK_Y	Enable/Disable X-channel tap event detection	0: X channel tap detection enabled (default) 1: X channel tap detection disabled
7	MASK_Z	Enable/Disable Z-channel tap event detection	0: Z channel tap detection enabled (default) 1: Z channel tap detection disabled

Table 53: Register 0x45 bit assignments

7.2.45(0X46,0X47) – FREEFALL THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x46	FreeFall Threshold LSB Register	FREEFALL_TH[7]	FREEFALL_TH[6]	FREEFALL_TH[5]	FREEFALL_TH[4]	FREEFALL_TH[3]	FREEFALL_TH[2]	FREEFALL_TH[1]	FREEFALL_TH[0]	0x00	R/W
0x47	FreeFall Threshold MSB Register	RESV	FREEFALL_TH[14]	FREEFALL_TH[13]	FREEFALL_TH[12]	FREEFALL_TH[11]	FREEFALL_TH[10]	FREEFALL_TH[9]	FREEFALL_TH[8]	0x00	R/W

Bit	Name	Function	Description
0x46 7:0	FREEFALL_TH[7:0]	Lower 8-bits of the Tap Latency Duration. The upper 7-bits are in register 0x47	Specifies the threshold below which a freefall event is detected. All channel values need to be below this threshold for a freefall event to be detected.
0x47 6:0	FREEFALL_TH[14:8]	Upper 7-bits of the Tap Latency Duration. The lower 8-bits are in register 0x46	
0x47 7	RESV	Reserved	Reserved

Table 54: Register 0x46/0x47 bit assignments

7.2.46 (0X48) – FREEFALL DURATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x48	FreeFall Duration Register	FREEFALL_ DUR[7]	FREEFALL _DUR[6]	FREEFALL _DUR[5]	FREEFALL _DUR[4]	FREEFALL _DUR[3]	FREEFALL _DUR[2]	FREEFALL _DUR[1]	FREEFAL L_DUR[0]	0x00	R/W

Bit	Name	Function	Description
7:0	FREEFALL_ DUR [7:0]	FreeFall Duration Count	The acceleration values for all 3 channels need to be below the freefall threshold value for at least the free fall duration for the event to be considered as a valid freefall event. This value is in terms of ODR or sample periods.

Table 55: Register 0x48 bit assignments

7.2.47(0X49,0X4A) – SIX DEGREES HIGH THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x49	SIXD High Threshold LSB Register	SIXD_HIGH_TH[7]	SIXD_HIGH_TH[6]	SIXD_HIGH_TH[5]	SIXD_HIGH_TH[4]	SIXD_HIGH_TH[3]	SIXD_HIGH_TH[2]	SIXD_HIGH_TH[1]	SIXD_HIGH_TH[0]	0x00	R/W
0x4A	SIXD High Threshold MSB Register	RESV	SIXD_HIGH_TH[14]	SIXD_HIGH_TH[13]	SIXD_HIGH_TH[12]	SIXD_HIGH_TH[11]	SIXD_HIGH_TH[10]	SIXD_HIGH_TH[9]	SIXD_HIGH_TH[8]	0x00	R/W

Bit	Name	Function	Description
0x49 7:0	SIXD_HIGH_TH [7:0]	Lower 8 bits of SIXD High Threshold LSB Register	Specifies the threshold above which an orientation event is detected. Two channels should have acceleration below the low threshold (SIXD_LOW_THRESH) and 1 channel should have acceleration above the threshold (SIXD_HIGH_THRESH) for the duration period (SIXD_DUR) to register an orientation change.
0x4A 6:0	SIXD_HIGH_TH [14:8]	Upper 7 bits of SIXD High Threshold MSB Register	
0x4A 7	RESV	Reserved	Reserved

Table 56: Register 0x49/0x4A bit assignments

7.2.48(0X4B,0X4C) – SIX DEGREES LOW THRESHOLD REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x4B	SIXD Low Threshold LSB Register	SIXD_LOW_TH[7]	SIXD_LOW_TH[6]	SIXD_LOW_TH[5]	SIXD_LOW_TH[4]	SIXD_LOW_TH[3]	SIXD_LOW_TH[2]	SIXD_LOW_TH[1]	SIXD_LOW_TH[0]	0x00	R/W
0x4C	SIXD Low Threshold MSB Register	RESV	SIXD_LOW_TH[14]	SIXD_LOW_TH[13]	SIXD_LOW_TH[12]	SIXD_LOW_TH[11]	SIXD_LOW_TH[10]	SIXD_LOW_TH[9]	SIXD_LOW _TH[8]	0x00	R/W

Bit	Name	Function	Description
0x4B 7:0	SIXD_LOW_TH [7:0]	Lower 8 bits of SIXD Low Threshold LSB Register	Specifies the threshold below which an orientation event is detected. Two channels should have acceleration below the low threshold (SIXD_LOW_THRESH) and 1 channel should have acceleration above the threshold (SIXD_HIGH_THRESH) for the duration period (SIXD_DUR) to register an orientation change.
0x4C 6:0	SIXD_ LOW _TH [14:8]	Upper 7 bits of SIXD Low Threshold MSB Register	
0x4C 7	RESV	Reserved	Reserved

Table 57: Register 0x4B/0x4C bit assignments

7.2.49(0X4D) – SIX DEGREE DURATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x4D	SIXD Duration Register	SIXD_DUR[7]	SIXD_DUR[6]	SIXD_DUR[5]	SIXD_DUR[4]	SIXD_DUR[3]	SIXD_DUR[2]	SIXD_DUR[1]	SIXD_DUR[0]	0x00	R/W

Bit	Name	Function	Description
0x4D 7:0	SIXD_DUR [7:0]	8-bit duration value for SIXD evaluation	Two channels should have acceleration below the low threshold (SIXD_LOW_THRESH) and 1 channel should have acceleration above the threshold (SIXD_HIGH_THRESH) for the duration period (SIXD_DUR) to register an orientation change. This duration count is in terms of ODR or sample periods.

Table 58: Register 0x4D bit assignments

7.2.50 (0X4E) – SIX DEGREES STATUS REGISTER

This read-only register reports the status of the SIXD orientation logic. Only one of the six bits below will be set to '1' at any time. Note that the power-on-reset value is dependent on the MXC3500AL orientation and operational mode.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x4E	SIXD Status Register	**RESV**	**RESV**	Z_NEG	Z_POS	X_NEG	X_POS	Y_NEG	Y_POS	0x00	RO

Bit	Name	Function	Description
0	Y_POS	Y-axis positive	0: System is not in Y_POS orientation 1: System is in Y_POS orientation
1	y_NEG	Y-axis negative	0: System is not in Y_NEG orientation 1: System is in Y_NEG orientation
2	X_POS	X-axis positive	0: System is not in X_POS orientation 1: System is in X_POS orientation
3	X_NEG	X-axis negative	0: System is not in X_NEG orientation 1: System is in X_NEG orientation
4	Z_POS	Z-axis positive	0: System is not in Z_POS orientation 1: System is in Z_POS orientation
5	Z_NEG	Z-axis negative	0: System is not in Z_NEG orientation 1: System is in Z_NEG orientation
6	RESV	Reserved	Reserved
7	RESV	Reserved	Reserved

Table 59: Register 0x4E bit assignments

7.2.51(0X50, 0X51) – INACTIVITY THRESHOLD REGISTER

This register is used specify the minimum threshold to determine when the accelermoter is inactive.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x50	Inactivity Threshold LSB	INACTIVITY_TH[7]	INACTIVITY_TH[6]	INACTIVITY_TH[5]	INACTIVITY_TH[4]	INACTIVITY_TH[3]	INACTIVITY_TH[2]	INACTIVITY_TH[1]	INACTIVITY_TH[0]	0x00	R/W
0x51	Inactivity Threshold MSB	INACTIVITY_ENB	INACTIVITY_TH[14]	INACTIVITY_TH[13]	INACTIVITY_TH[12]	INACTIVITY_TH[11]	INACTIVITY_TH[10]	INACTIVITY_TH[9]	INACTIVITY_TH[8]	0x00	R/W

Bit	Name	Function	Description
0x50 [7:0]	INACTIVITY_TH [7:0]	Inactivity Threshold LSB	Specifies the threshold below which inactivity is detected in WAKE mode. All channels should have acceleration below the inactivity threshold for the duration period (INACTIVITY_DUR, registers 0x52,0x53) to transition to SNIFF mode. The weighing of the threshold is approximately 0.7mg/bit.
0x51 [6:0]	INACTIVITY_TH [14:8]	Inactivity Threshold MSB	
0x51 [7]	INACTIVITY_ENB	Enables Inactivity Detection	0: Inactivity detection disabled (default) 1: Inactivity detection enabled

Table 60: Register 0x50/51 bit assignments

7.2.52(0X52,0X53) – INACTIVITY DURATION REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x52	Inactivity Duration Register LSB	INACTIVITY_DUR[7]	INACTIVITY_DUR[6]	INACTIVITY_DUR[5]	INACTIVITY_DUR[4]	INACTIVITY_DUR[3]	INACTIVITY_DUR[2]	INACTIVITY_DUR[1]	INACTIVITY_DUR[0]	0x00	R/W
0x53	Inactivity Duration Register MSB	INACTIVITY_DUR[15]	INACTIVITY_DUR[14]	INACTIVITY_DUR[13]	INACTIVITY_DUR[12]	INACTIVITY_DUR[11]	INACTIVITY_DUR[10]	INACTIVITY_DUR[9]	INACTIVITY_DUR[8]	0x00	R/W

Bit	Name	Function	Description
0x52 [7:0]	INACTIVITY_DUR [7:0]	Inactivity Duration Register LSB	Specifies the duration for which threshold should be below inactivity threshold for inactivity (registers 0x50,0x51) to be detected. All channels should have acceleration below the inactivity threshold for the duration period (INACTIVITY_DUR) to transition to SNIFF mode. This duration count is in terms of the ODR or sample periods.
0x53 [7:0]	INACTIVITY_DUR [15:8]	Inactivity Duration Register MSB	

Table 61: Register 0x52/53 bit assignments

7.2.53 (0X54) – WAKE CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x54	Wake Control Register **(WAKE_ CTRL_REG)**	SDM_WAIT _CNT[1]	SDM_WAIT _CNT[0]	SQ_OUT	**RESV**	INV_SDM_ CLK	OSR_SEL[2]	OSR_SEL[1]	OSR_SEL[0]	0x00	R/W

Bit	Name	Function	Description	
2:0	OSR_SEL[2:0]	Over Sampling Ratio Selection	This three-bit field selects the oversampling ratio for the SDM/main pipeline.	
			000	32
			001	64
			010	128
			011	256
			100	512
			101	1024
			110	2048
			111	4096
3	INV_SDM_ CLK	Inversion control for SDM clock	0: Clock to SDM is not inverted (default) 1: Clock to SDM is inverted.	
4	RESV	Reserved	Reserved	
5	SQ_OUT	Enable X^2+Y^2+Z^2 output in XYZ output registers.	0: SQ magnitude output is disabled (default) 1: SQ magnitude is output to registers 0x04 to 0x07. When this bit is '1' the 16-bit YOUT and ZOUT values are not available. Enabling this functionality captures X**2+Y**2+Z**2 in X and Y channel Output Register.	
7:6	SDM_WAIT_ CNT[1:0]	Specifies extra delay introduced before sampling Sigma Delta Input after enabling Sigma Delta	00 : 0 cycles 01 : 8 cycles 10 : 16 cycles 11 : 32 cycles	

Table 62: Register 0x54 bit assignments

7.2.54 (0X55) – RANGE CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x55	Range Control Register **(RANGE_ CTRL)**	**RESV**	RANGE[2]	RANGE[1]	RANGE[0]	**RESV**	**RESV**	**RESV**	**RESV**	0x00	R/W

Bit	Name	Function	Description		
3:0	RESV	Reserved	Reserved		
6:4	RANGE[3:0]	Set the accelerometer g-range scaling	This three-bit field accesses selects the resolution for the accelerometer.		Digital Scale factor
			000	+/-2g range (default)	12
			001	+/-4g range	6
			010	+/-8g range	3
			011	+/-16g range	3
			100	+/-12 range	2
			101	+/-24g range	1
			110	Not used	
			111	Not used	
7	RESV	Reserved	Reserved		

Table 63: Register 0x55 bit assignments

7.2.55 (0X56) – DECIMATION COUNT REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x56	Decimation Count Register **(DEC_CNT_REG)**	DECIMATION_CNT[7]	DECIMATION_CNT[6]	DECIMATION_CNT[5]	DECIMATION_CNT[4]	DECIMATION_CNT[3]	DECIMATION_CNT[2]	DECIMATION_CNT[1]	DECIMATION_CNT[0]	0x00	R/W

Bit	Name	Function	Description
7:0	DECIMATION_CNT[7:0]	Decimation count setting for main pipeline filters.	Software **must** set this value to 0x08 when the MXC3500AL is initialized.

Table 64: Register 0x56 bit assignments

7.2.56 (0X57) – WAKE CLOCK CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x57	WAKE Clock Control Register (**WAKE_CLOCK_CTRL_REG**)	**RESV**	**RESV**	**RESV**	SYS_OSC_FOSC[2]	SYS_OSC_FOSC[1]	SYS_OSC_FOSC[0]	SYS_OSC_NDIV[1]	SYS_OSC_NDIV[0]	0x1A	R/W

This register determines the clock settings when the MXC3500AL is in WAKE mode.

Bit	Name	Function	Description
1:0	SYS_OSC_NDIV[1:0]	Set the main oscillator divide by ratio for WAKE mode operations.	00: Selected main oscillator frequency is divided by 1 01: Selected main oscillator frequency is divided by 2 10: Selected main oscillator frequency is divided by 4 11: Selected main oscillator frequency is divided by 8 Bits 4:2 are used to select the main oscillator frequency. Bits 1:0 select the above divide by ratios.
4:2	SYS_OSC_FOSC[2:0]	Set the main oscillator frequency ratio for WAKE mode operations.	000: Main oscillator is 100 kHz 001: Main oscillator is 150 kHz 010: Main oscillator is 350 kHz 011: Main oscillator is 650 kHz 100: Main oscillator is 900 kHz 101: Main oscillator is 1.1 MHz 110: Main oscillator is 1.7 MHz 111: Main oscillator is 2.4 MHz
7:5	RESV	Reserved	Reserved

Table 65: Register 0x57 bit assignments

7.2.57 (0X59) – WAKE GCLK COUNT REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x59	Wake Burst Count (**WAKE_BURST_ COUNT**)	WK_BURST[7]	WK_BURST[6]	WK_BURST[5]	WK_BURST[4]	WK_BURST[3]	WK_BURST[2]	WK_BURST[1]	WK_BURST[0]	0xA0	R/W

Bit	Name	Function	Description
7:0	WK_BURST [7:0]	Set the number of clocks for the back-end pipeline.	This register should be set as instructed by Memsic.

Table 66: Register 0x59 bit assignments

7.2.58(0X5A,0X5B) – TIMESTAMP B0 REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x5A	Timestamp Bank 0 LSB **(TIMESTAMP_B0_LSB)**	TIMESTAMP_B0[7]	TIMESTAMP_B0[6]	TIMESTAMP_B0[5]	TIMESTAMP_B0[4]	TIMESTAMP_B0[3]	TIMESTAMP_B0[2]	TIMESTAMP_B0[1]	TIMESTAMP_B0[0]	0x00	RO
0x5B	Timestamp Bank 0 MSB **(TIMESTAMP_B0_MSB)**	TIMESTAMP_B0[15]	TIMESTAMP_B0[14]	TIMESTAMP_B0[13]	TIMESTAMP_B0[12]	TIMESTAMP_B0[11]	TIMESTAMP_B0[10]	TIMESTAMP_B0[9]	TIMESTAMP_B0[8]	0x00	RO

Bit	Name	Function	Description
15:0	TIMESTAMP_B0[15:0]	Timestamp Count for FIFO bank 0 or free running WAKE mode.	This value operates in two modes: • Non FIFO mode • FIFO ping-pong mode In non-FIFO mode, the timestamp value is updated each time a new sample is acquired. In FIFO ping-pong mode, this timestamp is an 16-bit unsigned count of when the first sample was written to an empty FIFO bank 0. This count is only used when the FIFO is enabled and operating in ping-pong mode. The local reset control for clearing the timestamp value is located at register 0x13 bit 5.

Table 67: Register 0x5A/5B bit assignments

7.2.59 (0X5C,0X5D) – TIMESTAMP B1 REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x5C	Timestamp Bank 1 LSB **(TIMESTAMP_B1_LSB)**	TIMESTAMP_B1[7]	TIMESTAMP_B1[6]	TIMESTAMP_B1[5]	TIMESTAMP_B1[4]	TIMESTAMP_B1[3]	TIMESTAMP_B1[2]	TIMESTAMP_B1[1]	TIMESTAMP_B1[0]	0x00	RO
0x5D	Timestamp Bank 1 MSB **(TIMESTAMP_B1_MSB)**	TIMESTAMP_B1[15]	TIMESTAMP_B1[14]	TIMESTAMP_B1[13]	TIMESTAMP_B1[12]	TIMESTAMP_B1[11]	TIMESTAMP_B1[10]	TIMESTAMP_B1[9]	TIMESTAMP_B1[8]	0x00	RO

Bit	Name	Function	Description
15:0	TIMESTAMP_B1[15:0]	Timestamp Count for FIFO bank 1	This timestamp is a 16-bit unsigned count of when the first sample was written to an empty FIFO bank 1. This count is only used when the FIFO is enabled and operating in ping-pong mode. The local reset control for clearing the timestamp value is located at register 0x13 bit 5.

Table 68: Register 0x5C/5D bit assignments

7.2.60 (0X5E) – TIMESTAMP CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x5E	Timestamp Control **(TIMESTAMP_CTRL)**	**RESV**	**RESV**	**RESV**	**RESV**	TS_CLK_ SEL[1]	TS_CLK_ SEL[0]	**RESV**	TIMESTAMP _EN	0x00	R/W

Bit	Name	Function	Description
0	TIMESTAMP_EN	Enable timestamp feature	0: Timestamp feature is disabled. 1: Timestamp feature is enabled. The local reset control for clearing the timestamp value is located at register 0x13 bit 5.
1	RESV	Reserved	Reserved
3:2	TS_CLK_SEL[1:0]	Timestamp counter clock select.	00: TS clock is system clock /4 01: TS clock is system clock /8 10: TS clock is system clock /16 11: TS clock is system clock /32
7:3	RESV	Reserved	Reserved

Table 69: Register 0x5E bit assignments

7.2.61 (0X60) – FIFO STATUS REGISTER 1

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x60	FIFO Status Register **(FIFO_STAT_1)**	FIFO_ WPTR[8]	FIFO_ RPTR[8]	FIFO_ SAMPLE_ CNT[8]	FIFO_ BANK1_FULL	FIFO_ BANK0_FULL	FIFO_THRESH	FIFO_FULL	FIFO_EMPTY	0x01	RO

Bit	Name	Function	Description
0	FIFO_EMPTY	FIFO empty flag	0: FIFO is not empty 1: FIFO is empty (default) This flag is valid if the FIFO is enabled or disabled. Note that this flag may change unexpectedly depending on FIFO reads or writes. This is a live flag bit and not latched.
1	FIFO_FULL	FIFO full flag	0: FIFO is not full (default) 1: FIFO is full This flag is valid if the FIFO is enabled or disabled. Note that this flag may change unexpectedly depending on FIFO reads or writes. This is a live flag bit and not latched.
2	FIFO_THRESH	FIFO threshold flag	0: FIFO threshold is less than threshold setting (default) 1: FIFO threshold is at or greater than threshold setting. Note that this flag may change unexpectedly depending on FIFO reads or writes. This is a live flag bit and not latched.
3	FIFO_ BANK0_FULL	FIFO bank 0 full flag	0: FIFO bank 0 is not full (default) 1: FIFO bank 0 is full
4	FIFO_ BANK1_FULL	FIFO bank 1 full flag	0: FIFO bank 1 is not full (default) 1: FIFO bank 1 is full
5	FIFO_ SAMPLE_ CNT[8]	FIFO sample count bit 8	MSB bit 8 of the FIFO sample count. The lower 8-bits are in register 0x63.
6	FIFO_ RPTR[8	FIFO read pointer bit 8	MSB bit 8 of the FIFO read pointer. The lower 8-bits are in register 0x61.
7	FIFO_ WPTR[8]	FIFO write pointer bit 8	MSB bit 8 of the FIFO write pointer. The lower 8-bits are in register 0x62.

Table 70: Register 0x60 bit assignments

7.2.62(0X61) – FIFO STATUS REGISTER 2

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x61	FIFO Read Pointer **(FIFO_STAT_2)**	FIFO_RPTR[7]	FIFO_RPTR[6]	FIFO_RPTR[5]	FIFO_RPTR[4]	FIFO_RPTR[3]	FIFO_RPTR[2]	FIFO_RPTR[1]	FIFO_RPTR[0]	0x00	RO

Bit	Name	Function	Description
7:0	FIFO_RPTR[7:0]	Lower 8-bits of the FIFO read pointer	The FIFO read pointer is a 9-bit value that points to the current address of the read port on the FIFO. The actual address are bits 7:0 since the FIFO is limited to 256. Bit 8 (register 0x60 bit 6) is used as “wrap” flag by hardware when comparing the read and write pointers.

Table 71: Register 0x61 bit assignments

7.2.63(0X62) – FIFO STATUS REGISTER 3

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x62	FIFO Write Pointer **(FIFO_STAT_3)**	FIFO_ WPTR[7]	FIFO_ WPTR[6]	FIFO_ WPTR[5]	FIFO_ WPTR[4]	FIFO_ WPTR[3]	FIFO_ WPTR[2]	FIFO_ WPTR[1]	FIFO_ WPTR[0]	0x00	RO

Bit	Name	Function	Description
7:0	FIFO_WPTR[7:0]	Lower 8-bits of the FIFO write pointer	The FIFO write pointer is a 9-bit value that points to the current address of the write port on the FIFO. The actual address are bits 7:0 since the FIFO is limited to 256 samples. Bit 8 (register 0x60 bit 7) is used as "wrap" flag by hardware when comparing the read and write pointers.

Table 72: Register 0x62 bit assignments

7.2.64 (0X63) – FIFO STATUS REGISTER 4

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x63	FIFO Sample Count **(FIFO_STAT_4)**	FIFO_SAMPLE_CNT[7]	FIFO_SAMPLE_CNT[6]	FIFO_SAMPLE_CNT[5]	FIFO_SAMPLE_CNT[4]	FIFO_SAMPLE_CNT[3]	FIFO_SAMPLE_CNT[2]	FIFO_SAMPLE_CNT[1]	FIFO_SAMPLE_CNT[0]	0x00	RO

Bit	Name	Function	Description
7:0	FIFO_SAMPLE_CNT [7:0]	Lower 8-bits of the FIFO sample count	The FIFO sample count is a 9-bit value that reports the current number of samples in the FIFO. The FIFO address ranges from 0x00 to 0xFF (0 to 255). Note that bit 8 of the FIFO sample count is in register 0x60 bit 6. The sample count is the delta between the read and write pointers in the FIFO. This value may change unexpectedly with respect to FIFO writes or serial communications, so it should be used as an indication of FIFO capacity and not an absolute sample count.

Table 73: Register 0x63 bit assignments

7.2.65(0X64-0X6D) – LPF COEFFICIENT REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x64	XL LPF Coefficient B0 LSB	X_LPF_B0[7]	X_LPF_B0[6]	X_LPF_B0[5]	X_LPF_B0[4]	X_LPF_B0[3]	X_LPF_B0[2]	X_LPF_B0[1]	X_LPF_B0[0]	0x00	R/W
0x65	XL LPF Coefficient B0 MSB	X_LPF_B0[15]	X_LPF_B0[14]	X_LPF_B0[13]	X_LPF_B0[12]	X_LPF_B0[11]	X_LPF_B0[10]	X_LPF_B0[9]	X_LPF_B0[8]	0x00	R/W
0x66	XL LPF Coefficient B1 LSB	X_LPF_B1[7]	X_LPF_B1[6]	X_LPF_B1[5]	X_LPF_B1[4]	X_LPF_B1[3]	X_LPF_B1[2]	X_LPF_B1[1]	X_LPF_B1[0]	0x00	R/W
0x67	XL LPF Coefficient B1 MSB	X_LPF_B1[15]	X_LPF_B1[14]	X_LPF_B1[13]	X_LPF_B1[12]	X_LPF_B1[11]	X_LPF_B1[10]	X_LPF_B1[9]	X_LPF_B1[8]	0x00	R/W
0x68	XL LPF Coefficient B2 LSB	X_LPF_B2[7]	X_LPF_B2[6]	X_LPF_B2[5]	X_LPF_B2[4]	X_LPF_B2[3]	X_LPF_B2[2]	X_LPF_B2[1]	X_LPF_B2[0]	0x00	R/W
0x69	XL LPF Coefficient B2 MSB	X_LPF_B2[15]	X_LPF_B2[14]	X_LPF_B2[13]	X_LPF_B2[12]	X_LPF_B2[11]	X_LPF_B2[10]	X_LPF_B2[9]	X_LPF_B2[8]	0x00	R/W
0x6A	XL LPF Coefficient A1 LSB	X_LPF_A1[7]	X_LPF_A1[6]	X_LPF_A1[5]	X_LPF_A1[4]	X_LPF_A1[3]	X_LPF_A1[2]	X_LPF_A1[1]	X_LPF_A1[0]	0x00	R/W
0x6B	XL LPF Coefficient A1 MSB	X_LPF_A1[15]	X_LPF_A1[14]	X_LPF_A1[13]	X_LPF_A1[12]	X_LPF_A1[11]	X_LPF_A1[10]	X_LPF_A1[9]	X_LPF_A1[8]	0x00	R/W
0x6C	XL LPF Coefficient A2 LSB	X_LPF_A2[7]	X_LPF_A2[6]	X_LPF_A2[5]	X_LPF_A2[4]	X_LPF_A2[3]	X_LPF_A2[2]	X_LPF_A2[1]	X_LPF_A2[0]	0x00	R/W
0x6D	XL LPF Coefficient A2 MSB	X_LPF_A2[15]	X_LPF_A2[14]	X_LPF_A2[13]	X_LPF_A2[12]	X_LPF_A2[11]	X_LPF_A2[10]	X_LPF_A2[9]	X_LPF_A2[8]	0x00	R/W

Please contact Memsic for coefficient settitngs.

Bit	Name	Function	Description
0x64 7:0 **0x65 7:0**	XL LPF Coefficient B0 LSB/MSB	16-bit value for LPF coefficient B0 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements.
0x66 7:0 **0x67 7:0**	XL LPF Coefficient B1 LSB/MSB	16-bit value for LPF coefficient B1 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements.
0x68 7:0 **0x69 7:0**	XL LPF Coefficient B2 LSB/MSB	16-bit value for LPF coefficient B2 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements.
0x6A 7:0 **0x6B 7:0**	XL LPF Coefficient A1 LSB/MSB	16-bit value for LPF coefficient A1 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements. This value is always considered a negative coefficient by the filter hardware.
0x6C 7:0 **0x6D 7:0**	XL LPF Coefficient A2 LSB/MSB	16-bit value for LPF coefficient A2 (unsigned)	This coefficient may be changed to match different ODR/sample rates and BW requirements.

Table 74: Register 0x64-0x6D bit assignments

7.2.66(0X6E) – LPF CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x6E	LPF Control Register	**RESV**	**RESV**	**RESV**	**RESV**	**RESV**	LPF_RESET	LPF_PASS_ THROUGH	LPF_EN	0x00	R/W

Bit	Name	Function	Description
0	LPF_EN	Enable/Disable the Low Pass Filter.	0: low pass filter is disabled. 1: low pass filter is enabled (adds a 2-sample delay)
1	LPF_PASS_ THROUGH	Enable pass through mode for LPF, all coefficients are set to '1'.	0: LPF pass thru mode is disabled (requires coefficients be programmed). 1: LPF pass thru mode is enabled (does not require coefficients)
2	LPF_RESET	Low pass filter local reset	0: Filter reset is not applied. 1: Filter is held in reset (level). It is highly recommended to reset the LPF whenever coefficients are updated or changed.
7:3	RESV	Reserved	Reserved

Table 75: Register 0x6E bit assignments

7.2.67 (0X7F) – RESET REGISTER

Addr	Name	Description	Bit								POR Value	R/W
			7	6	5	4	3	2	1	0		
0x7F	RESET_ REG	Reset Register	SW_ RESET	RESV	RESV	RESV	RESV	RESV	RESV	RESV	0x00	RW

Bit	Name	Function	Description
6:0	RESV	RESERVED	Reserved.
7	SW_RESET	Software controlled reset.	0: Soft reset is disabled (default). 1: Software reset is enabled. This active high reset will trigger a complete reboot of the MXC3500AL. All registers will be reloaded with OTP defaults or power-on-reset defaults. This bit is self clearing.

Table 76: Register 0x7F bit assignments

7.2.68(0X80-0X85) – MAIN OFFSET REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x80	**XL_MN_YOFFL**	MN_ YOFFL[7]	MN_ YOFFL[6]	MN_ YOFFL[5]	MN_ YOFFL[4]	MN_ YOFFL[3]	MN_ YOFFL[2]	MN_ YOFFL[1]	MN_ YOFFL[0]	OTP	R/W
0x81	**XL_MN_YOFFH**	RESV	MN_ YOFFH[14]	MN_ YOFFH[13]	MN_ YOFFH[12]	MN_ YOFFH[11]	MN_ YOFFH[10]	MN_ YOFFH[9]	MN_ YOFFH[8]	OTP	R/W
0x82	**XL_MN_XOFFL**	MN_ XOFFL[7]	MN_ XOFFL[6]	MN_ XOFFL[5]	MN_ XOFFL[4]	MN_ XOFFL[3]	MN_ XOFFL[2]	MN_ XOFFL[1]	MN_ XOFFL[0]	OTP	R/W
0x83	**XL_MN_XOFFH**	RESV	MN_ XOFFH[14]	MN_ XOFFH[13]	MN_ XOFFH[12]	MN_ XOFFH[11]	MN_ XOFFH[10]	MN_ XOFFH[9]	MN_ XOFFH[8]	OTP	R/W
0x84	**XL_MN_ZOFFL**	MN_ ZOFFL[7]	MN_ ZOFFL[6]	MN _ZOFFL[5]	MN_ ZOFFL[4]	MN_ ZOFFL[3]	MN_ ZOFFL[2]	MN_ ZOFFL[1]	MN_ ZOFFL[0]	OTP	R/W
0x85	**XL_MN_ZOFFH**	RESV	MN_ ZOFFH[14]	MN_ ZOFFH[13]	MN_ ZOFFH[12]	MN_ ZOFFH[11]	MN_ ZOFFH[10]	MN_ ZOFFH[9]	MN_ ZOFFH[8]	OTP	R/W

Bit	Name	Function	Description
0x80 7:0 **0x81 6:0**	XL Main Y-axis Offset LSB/MSB	Y-axis, main pipeline digital offset adjustment	This is a signed 2's complement 15-bit value applied as an offset adjustment to the corresponding XL channel. This is a factory trimmed parameter; please contact Memsic before modifying.
0x82 7:0 **0x83 6:0**	XL Main X-axis Offset LSB/MSB	X-axis, main pipeline digital offset adjustment	This is a signed 2's complement 15-bit value applied as an offset adjustment to the corresponding XL channel. This is a factory trimmed parameter; please contact Memsic before modifying.
0x84 7:0 **0x85 6:0**	XL Main Z-axis Offset LSB/MSB	Z-axis, main pipeline digital offset adjustment	This is a signed 2's complement 15-bit value applied as an offset adjustment to the corresponding XL channel. This is a factory trimmed parameter; please contact Memsic before modifying.

Table 77: Register 0x80-0x85 bit assignments

7.2.69(0X86-0X8B) – MAIN GAIN REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x86	**MN_YGAINL**	MN_ YGAIN[7]	MN_ YGAIN[6]	MN_ YGAIN[5]	MN_ YGAIN[4]	MN_ YGAIN[3]	MN_ YGAIN[2]	MN_ YGAIN[1]	MN_ YGAIN[0]	OTP	R/W
0x87	**MN_YGAINH**	**RESV**	**RESV**	**RESV**	SN_ TGAIN[8]	SN_ ZGAIN[8]	SN_ YGAIN[8]	SN_ YGAIN[8]	MN_ YGAIN[8]	OTP	R/W
0x88	**MN_XGAINL**	MN_ XGAIN[7]	MN_ XGAIN[6]	MN_ XGAIN[5]	MN_ XGAIN[4]	MN_ XGAIN[3]	MN_ XGAIN[2]	MN_ XGAIN[1]	MN_ XGAIN[0]	OTP	R/W
0x89	**MN_XGAINH**	**RESV**	**RESV**	**RESV**	**RESV**	**RESV**	**RESV**	**RESV**	MN_ XGAIN[8]	OTP	R/W
0x8A	**MN_ZGAINL**	MN_ ZGAIN[7]	MN_ ZGAIN[6]	MN_ ZGAIN[5]	MN_ ZGAIN[4]	MN_ ZGAIN[3]	MN_ ZGAIN[2]	MN_ ZGAIN[1]	MN_ ZGAIN[0]	OTP	R/W
0x8B	**MN_ZGAINH**	**RESV**	**RESV**	**RESV**	**RESV**	**RESV**	**RESV**	**RESV**	MN_ ZGAIN[8]	OTP	R/W

Bit	Name	Function	Description
0x86 7:0 0x87 0	XL Main X-axis Gain LSB/MSB	X-axis, main pipeline digital gain adjustment	This 9-bit unsigned value applies a digital gain to the corresponding XL channel. This is a factory trimmed parameter; do not modify unless instructed by Memsic.
0x88 7:0 0x89 0	XL Main Y-axis Gain LSB/MSB	Y-axis, main pipeline digital gain adjustment	This 9-bit unsigned value applies a digital gain to the corresponding XL channel. This is a factory trimmed parameter; do not modify unless instructed by Memsic.
0x8A 7:0 0x8B 0	XL Main Z-axis Gain LSB/MSB	Z-axis, main pipeline digital gain adjustment	This 9-bit unsigned value applies a digital gain to the corresponding XL channel. This is a factory trimmed parameter; do not modify unless instructed by Memsic.

Table 78: Register 0x86-0x8B bit assignments

7.2.70(0X8C-0X8F) – SNIFF OFFSET REGISTERS

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x8C	**SN_YOFF**	SN_ YOFF[7]	SN_ YOFF[6]	SN_ YOFF[5]	SN_ YOFF[4]	SN_ YOFF[3]	SN_ YOFF[2]	SN_ YOFF[1]	SN_ YOFF[0]	OTP	R/W
0x8D	**SN_XOFF**	SN_ XOFF[7]	SN_ XOFF[6]	SN_ XOFF[5]	SN_ XOFF[4]	SN_ XOFF[3]	SN_ XOFF[2]	SN_ XOFF[1]	SN_ XOFF[0]	OTP	R/W
0x8E	**SN_ZOFF**	SN_ ZOFF[7]	SN_ ZOFF[6]	SN_ ZOFF[5]	SN_ ZOFF[4]	SN_ ZOFF[3]	SN_ ZOFF[2]	SN_ ZOFF[1]	SN_ ZOFF[0]	OTP	R/W
0x8F	**SN_TOFF**	SN_ TOFF[7]	SN_ TOFF[6]	SN_ TOFF[5]	SN_ TOFF[4]	SN_ TOFF[3]	SN_ TOFF[2]	SN_ TOFF[1]	SN_ TOFF[0]	OTP	R/W

Bit	Name	Function	Description
0x8C	Sniff Y-axis Offset	Y-axis, sniff pipeline digital offset	This is a factory trimmed parameter. Do not modify unless advised by Memsic.
0x8D	Sniff X-axis Offset	X-axis, sniff pipeline digital offset	This is a factory trimmed parameter. Do not modify unless advised by Memsic.
0x8E	Sniff Z-axis Offset	Z-axis, sniff pipeline digital offset	This is a factory trimmed parameter. Do not modify unless advised by Memsic.
0x8F	Sniff T-channel Offset	T-channel, sniff pipeline digital offset	This is a factory trimmed parameter. Do not modify unless advised by Memsic.

Table 79: Register 0x8C/0x8D/0x8E/0x8F bit assignments

7.2.71(0X90-0X93) – SNIFF GAIN REGISTERS

The SNIFF gain registers are values applied to the X, Y, Z and T channels.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x87	**MN_XGAINH**	**RESV**	**RESV**	**RESV**	SN_ TGAIN[8]	SN_ ZGAIN[8]	SN_ XGAIN[8]	SN_ YGAIN[8]	MN_ YGAIN[8]	OTP	R/W
0x90	**SN_YGAIN**	SN_ YGAIN[7]	SN_ YGAIN[6]	SN_ YGAIN[5]	SN_ YGAIN[4]	SN_ YGAIN[3]	SN_ YGAIN[2]	SN_ YGAIN[1]	SN_ YGAIN[0]	OTP	R/W
0x91	**SN_XGAIN**	SN_ XGAIN[7]	SN_ XGAIN[6]	SN_ XGAIN[5]	SN_ XGAIN[4]	SN_ XGAIN[3]	SN_ XGAIN[2]	SN_ XGAIN[1]	SN_ XGAIN[0]	OTP	R/W
0x92	**SN_ZGAIN**	SN_ ZGAIN[7]	SN_ ZGAIN[6]	SN_ ZGAIN[5]	SN_ ZGAIN[4]	SN_ ZGAIN[3]	SN_ ZGAIN[2]	SN_ ZGAIN[1]	SN_ ZGAIN[0]	OTP	R/W
0x93	**SN_TGAIN**	SN_ TGAIN[7]	SN_ TGAIN[6]	SN_ TGAIN[5]	SN_ TGAIN[4]	SN_ TGAIN[3]	SN_ TGAIN[2]	SN_ TGAIN[1]	SN_ TGAIN[0]	OTP	R/W

Bit	Name	Function	Description
0x87 bit 1 0x90 bits 7:0	Sniff Y-axis Gain	Y-axis, sniff pipeline digital gain	9-bit unsigned value applies a digital gain to the corresponding XL channel. This is a factory trim parameter. Do not modify unless instructed by Memsic.
0x87 bit 2 0x91 bits 7:0	Sniff X-axis Gain	X-axis, sniff pipeline digital gain	
0x87 bit 3 0x92 bits 7:0	Sniff Z-axis Gain	Z-axis, sniff pipeline digital gain	
0x87 bit 4 0x93 bits 7:0	Sniff T-channel Gain	T-channel, sniff pipeline digital gain	

Table 80: Register 0x87/0x90/0x91/0x92/0x93 bit assignments

7.2.72 (0X94) – POLARITY REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x94	XL Polarity Register (POL_REG)	SAR_ POL_T	SAR_ POL_Z	SAR_ POL_X	SAR_ POL_Y	RESV	SDM_ Z_POL	SDM_ X_POL	SDM_ Y_POL	OTP	R/W

This is a factory trim parameter. Do not modify unless instructed by Memsic.

Bit	Name	Function	Description
0	SDM_ Y_POL	Y-axis polarity, SDM ADC	0: Y-axis data from SDM is not inverted (default) 1: Y-axis data from SDM is inverted
1	SDM_ X_POL	Y-axis polarity, SDM ADC	0: X-axis data from SDM is not inverted (default) 1: X-axis data from SDM is inverted
2	SDM_ Z_POL	X-axis polarity, SDM ADC	0: Z-axis data from SDM is not inverted (default) 1: Z-axis data from SDM is inverted
3	RESV	Reserved	Reserved
4	SAR_ POL_Y	Y-axis polarity, SAR ADC	0: Y-axis data from SAR is not inverted (default) 1: Y-axis data from SAR is inverted
5	SAR_ POL_X	X-axis polarity, SAR ADC	0: X-axis data from SAR is not inverted (default) 1: X-axis data from SAR is inverted
6	SAR_ POL_Z	Z-axis polarity, SAR ADC	0: Z-axis data from SAR is not inverted (default) 1: Z-axis data from SAR is inverted
7	SAR_ POL_T	T-channel polarity, SAR ADC	0: T-channel data from SAR is not inverted (default) 1: T-channel from SAR is inverted

Table 81: Register 0x94 bit assignments

7.2.73(0X9B) – SAR OFFSET SHIFT REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x9B	SAR_OFFSET_SHIFT_XYZ	SAR_OFFSET_SHIFT_XYZ[7]	SAR_OFFSET_SHIFT_XYZ[6]	SAR_OFFSET_SHIFT_XYZ[5]	SAR_OFFSET_SHIFT_XYZ[4]	SAR_OFFSET_SHIFT_XYZ[3]	SAR_OFFSET_SHIFT_XYZ[2]	SAR_OFFSET_SHIFT_XYZ[1]	SAR_OFFSET_SHIFT_XYZ[0]	OTP	R/W

Bit	Name	Function	Description
7:0	SAR_OFFSET_SHIFT_XYZ	8-bit SAR offset adjustment for XYZ channel measurements.	This 8-bit value can be applied as an offset adjustment to the SAR ADC when sampling X, Y, or Z-axis values. This value is applied when register 0x20 bit 3, "SAR_OFFSET_MODE" is set to a '1'.

Table 82: Register 0x9B bit assignments

7.2.74(0X9C) – SAR OFFSET SHIFT TEMP REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x9C	SAR OFFSET SHIFT Register (TEMP)	SAR_OFFSET_SHIFT_TEMP[7]	SAR_OFFSET_SHIFT_TEMP[6]	SAR_OFFSET_SHIFT_TEMP[5]	SAR_OFFSET_SHIFT_TEMP[4]	SAR_OFFSET_SHIFT_TEMP[3]	SAR_OFFSET_SHIFT_TEMP[2]	SAR_OFFSET_SHIFT_TEMP[1]	SAR_OFFSET_SHIFT_TEMP[0]	OTP	R/W

Bit	Name	Function	Description
7:0	SAR_OFFSET_SHIFT_TEMP	8-bit SAR offset adjustment for Temp channel measurements.	This 8-bit value can be applied as an offset adjustment to the SAR ADC when sampling the T-channel. This value is applied when register 0x20 bit 3, "SAR_OFFSET_MODE" is set to a '1'.

Table 83: Register 0x9C bit assignments

7.2.75 (0X9E) – VTRIM REFERENCE REGISTER

This register holds the factory trim value for the voltage reference. Do not modify this value unless instructed by Memsic.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x9E	VTRIM Reference Register (VTRIM_REF_REG)	RESV	RESV	RESV	RESV	VTRIM_REF [3]	VTRIM_REF [2]	VTRIM_REF [1]	VTRIM_REF [0]	OTP	R/W

Bit	Name	Function	Description
3:0	VTRIM_REF[3:0]	Voltage reference trim.	This unsigned value sets the trim level for the voltage reference. The value of the digital LDO (DLDO) is determined by this setting. 0x0: max Vref level 0x8: mid Vref level (default) 0xF: min Vref level This value is factory trim and OTP backed.
7:4	RESV	Reserved	Reserved

Table 84: Register 0x9E bit assignments

7.2.76 (0X9F) – RBIAS REFERENCE TRIM REGISTER

This register holds the factory trim value for the reference current generator. Do not modify this value unless instructed by Memsic.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x9F	RBIAS Reference Register (RBIAS_REF_REG)	RESV	RESV	RBIAS_REF [5]	RBIAS_REF [4]	RBIAS_REF [3]	RBIAS_REF [2]	RBIAS_REF [1]	RBIAS_REF [0]	OTP	R/W

Bit	Name	Function	Description
5:0	RBIAS_REF [5:0]	RBIAS reference trim.	This is an unsigned 6-bit trim value. Note that the minimum trim code corresponds to the largest current. Weighting is approximately 4nA/bit. 0x00: Maximum bias current (280nA) 0x3F: Minimum bias current (25nA) This value is factory trim and OTP backed.
7:6	RESV	Reserved	Reserved

Table 85: Register 0x9F bit assignments

7.2.77(0XB6) – WAKE IBSEL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0xB6	WAKE_IBSEL_CTRL_REG	RESV	RESV	IBSEL[5]	IBSEL[4]	IBSEL[3]	IBSEL[2]	IBSEL[1]	IBSEL[0]	0x11	R/W

The IBSEL value (IBIAS select) sets reference currents for parts of the analog. During boot and power-up the value is held by hardware so that all parts of the device initialize correctly. Some settings are tentative pending device characterization. Please contact Memsic for additional information.

Bit	Name	Function	Description
5:0	WAKE_IBSEL[5:0]	IB selection bits for use in WAKE mode operations.	0x00: Minimum value, approximately 1nA 0x11: Default value, approximately 17nA 0x3F: Maximum value, approximately 64nA Step size for the IBSEL value is 1nA/LSB.
7:6	RESV	Reserved	Reserved

Table 86: Register 0xB6 bit assignments

7.2.78 (0XB7) – LDO CONTROL REGISTER

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0xB7	LDO_CTRL REG	IBSEL_ LOW[1]	IBSEL_ LOW[0]	RESV	INPUT_ SELECT_ BOOST_EN	VSEL_ ALDO[1]	VSEL_ ALDO[0]	ALDO_EN	RESV	0x02	R/W

Bit	Name	Function	Description
0	RESV	Reserved	Reserved
1	ALDO_EN		0: ALDO is disabled 1: ALDO is enabled (default)
3:2	SEL_ALDO[1:0]	Analog LDO voltage select	These two bits control the voltage level of the analog regulator (ALDO). The default value is same as the DLDO, or 1.0V. If the ALDO is set to 1.25V, the external VDD level must be set to 1.5V If the ALDO is set to 1.5V, the external VDD level must be set to 1.7V 00: 1.0V output (default) 01: 1.25V output (requires external VDD to be 200mV higher or 1.5V) 10: 1.25V output (requires external VDD to be 200mV higher or 1.5V) 11: 1.50V output (requires external VDD to be 200mV higher or 1.7V)
4	INPUT_SELECT_ BOOST_EN	Boost select for SAR operation.	0: Input boost select is disabled (default). 1: Input boost select is enabled.
5	RESV	Reserved	Reserved
7:6	IBSEL_LOW[1:0]	Low power IBSEL control for SDM	This controls an extra low power mode for the SDM (not SAR). The IBSEL[5:0] value affected by this setting is in register 0xB6 (WAKE IBSEL setting). 00: 100% of IBSEL[5:0] flows to SDM ibias. 01: 66% of IBSEL[5:0] flows to SDM ibias. 10: 66% of IBSEL[5:0] flows to SDM ibias. 11: 33% of IBSEL[5:0] flows to SDM ibias.

Table 87: Register 0xB7 bit assignments

8 TABLES AND FIGURES

9 REVISION HISTORY

Date	Revision	Description
2021-02	Preliminary	Preliminary version for review internally
2021-03	Preliminary Update 1	Update application circuits and operational currents
2021-04	Preliminary Update 2	Update figures and register summary
2021-05	Preliminary Update 3	Fix various typos.
2021-06	Preliminary Update 4	Update operational currents.
2021-10	Preliminary Update 5	Update ordering information
2021-11	Preliminary Update 6	Update specifications. Added details on Range block
2021-11	Preliminary Update 7	Clarified register POR defaults, new register information.
2021-11-24	V1.00	Release version 1.00
2021-12-01	V1.02	Update.
2022-01-20	V1.03	Update.
2022-04-01	V1.04	Update.

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